











THIRD INTERIM PROGRESS REPORT  
ON THE  
PHYSICAL REALIZATION OF AN  
ELECTRONIC COMPUTING INSTRUMENT

by

Julian H. Bigelow  
Theodore W. Hildebrandt  
James H. Pomerene  
Jack Rosenberg  
Ralph J. Slutz  
Willis H. Ware

The Institute for Advanced Study  
Princeton, New Jersey

1 January 1949

(Reprinted September 1950)





INTERIM . . .

THIRD

INTERIM PROGRESS REPORT

ON THE

PHYSICAL REALIZATION OF AN

ELECTRONIC COMPUTING INSTRUMENT

By

Julian H. Bigelow  
Theodore W. Hildebrandt  
James H. Pomerene  
Jack Rosenberg  
Ralph J. Slutz  
Willis H. Ware

IAS ECP list of reports,  
1946-57. no. 7.

Institute for Advanced Study

1 January 1948



# TABLE OF CONTENTS

	Page
Preface . . . . .	4
I. Summary . . . . .	6
II. Introduction . . . . .	8
III. Input-Output-Organs . . . . .	10
A. Electronic Equipment . . . . .	10
1. Input recording equipment . . . . .	10
2. Input distributor rack . . . . .	14
3. Equipment for transcribing from inner memory to wire . . . . .	21
4. Equipment for transcribing from wire to teletype tape . . . . .	24
B. Mechanical Equipment . . . . .	25
1. Teletype equipment . . . . .	25
2. High-speed wire drive . . . . .	25
C. Record Reproduce Tests . . . . .	35
1. New brush wire . . . . .	35
2. Tests with loop drive . . . . .	35
3. Tests with the high-speed drive . . . . .	38
D. Additional Marker Pulses . . . . .	40
IV. Arithmetic Organs. . . . .	47
A. Shifting Register . . . . .	47
1. Register No. 1. (Conditional clear type shifting register) . . . . .	47
2. Register No. 3 . . . . .	53
3. Single vs. double registers . . . . .	68
B. Accumulators . . . . .	77
1. Accumulator No. 2. (Double Kirchhoff summation type). . . . .	78
2. Accumulator No. 7 . . . . .	82
V. Control Organs . . . . .	111
A. Pulsers . . . . .	112
1. Pulser No. 1 . . . . .	112
2. Pulser No. 2 . . . . .	116
B. Counters . . . . .	119
1. Binary Counter No. 1 . . . . .	126
2. Binary Counter No. 2 . . . . .	128
C. Multiplier No. 1 . . . . .	139
VI. Laboratory Equipment . . . . .	146

# PHOTOGRAPHS

	Page
1. Erasing Oscillator and Recording Driver . . . . .	16
2. Limiter, Shaper, and Selector Chassis	
a. Front view . . . . .	17
b. Rear view . . . . .	17
3. High-Speed Wire Drive No. 3	
a. Wire reels in place . . . . .	31
b. Index mechanism for wire reels . . . . .	31
c. Index pins of wire reels . . . . .	32
d. Tachometer, drive pulley, and slip rings . . . . .	32
e. Assembly showing traverse system . . . . .	33
f. Assembly showing drive and power auxiliaries . . . . .	34
4. Oscillogram of Word	
a. Reproduced directly from magnetic wire . . . . .	37
b. After limiting . . . . .	37
5. Accumulator No. 7	
a. Complete unit . . . . .	102
b. Adding circuits . . . . .	102
c. Digit recording gates . . . . .	103
d. Shifting register . . . . .	103
6. Pulser No. 1. . . . .	114
7. Pulser No. 2 attached to Quadruple Variable Pulser . . . . .	118
8. Binary Counter No. 2 . . . . .	135
9. Multiplier No. 1 and Power Supply . . . . .	140
10. Regulated Motor-Generator No. 1	
a. General view . . . . .	147
b. Regulator chassis . . . . .	147
11. Converted Regulated Power Supply . . . . .	148
12. Power Supplies for Accumulator No. 7	
a. For adding circuits . . . . .	149
b. For shifting register . . . . .	149
13. 1500 Volt, 200 MA. Power Supply . . . . .	150

# DRAWINGS

	Page
C-3-1009-I	Recording Driver No. 2 . . . . . 12
C-3-1023	Erasing Oscillator . . . . . 15
C-3-1002-D	Input Distributor . . . . . 19
C-3-1002-G	Input Distributor . . . . . 20
C-2-1026	One Ampere Voltage Regulator . . . . . 22
C-3-1032	High-Speed Recording Control Circuit . . . . . 23
C-2-1027	Pulse Group Generator No. 2 . . . . . 48
C-3-1028	Gating System of Register No. 1 . . . . . 51
C-3-1029	Shifting Register No. 3 . . . . . 55
C-3-1021	Shifting Register No. 3 . . . . . 56
C-3-1030	Auxiliary Circuits for Register No. 3 . . . . . 62
C-3-1031	Pulses for Register No. 3 . . . . . 64
C-3-1034	Optimum Register Types . . . . . 75
C-3-1033	Cycle Times for Single and Double Resistors . . . . . 76
C-3-1022	Adding Circuits of Accumulator No. 7 . . . . . 92
C-3-1025	Digit Recording Gates No. 1 . . . . . 107
C-3-1027	Clamping Circuit for Pulsed Toggle Grid . . . . . 109
C-3-1026	Trigger, Blocking Oscillators and Output Cathode Follower . . . . . 113
C-3-1024	Blocking Oscillator . . . . . 117
C-3-1035	Pulses from Pulser No. 2 . . . . . 120
C-3-1041	Eccles-Jordan Toggle Stage . . . . . 121
C-3-1042	Counter No. 1. . . . . 127
C-3-1040	Block Diagram of a Gated Counter . . . . . 129
C-3-1036	Block Diagram of a Counter No. 2 . . . . . 131
C-3-1037	Counter No. 2. . . . . 133
C-3-1038	Operating Zones for Counter Gates . . . . . 134
C-3-1039	Revised Schematic of Counter No. 2 . . . . . 138
C-3-1044	Delay Circuit . . . . . 143
C-3-1043	Gating Unit of Multiplier No. 1 . . . . . 144
C-2-1020	High-range Voltage Regulator . . . . . 151
C-2-1021	Low-range Voltage Regulator . . . . . 152
C-2-1023	800 Volt Voltage Regulator . . . . . 153
C-2-1024	400 Volt Voltage Regulator . . . . . 154
C-2-1025	1000 to 1500 Volt Power Supply . . . . . 155
C-2-1015	Sweep, Marker, and Trigger Generator Chassis . . . . . 156

## P R E F A C E

The ensuing report has been prepared in accordance with the terms of contract W-36-034-ORD-7481 between the Research and Development Service, Ordnance Department, Department of the Army, and the Institute for Advanced Study. The express purpose of this report is to furnish contemporary advice to the Service regarding steps taken and contemplated toward the realization of an electronic computing instrument embodying the principles outlined in the following Institute for Advanced Study reports:

28 June 1946, by Burks, Goldstine, and von Neumann entitled: "Preliminary Discussion of the Logical Design of an Electronic Computing Instrument ." (Hereinafter referred to as Logical Design Report No. 1)

1 January 1947, by Bigelow, Pomerene, Slutz, and Ware entitled: "Interim Progress Report on the Physical Realization of an Electronic Computing Instrument." (Hereinafter referred to as Progress Report No. 1)

1 April 1947, by Goldstine and von Neumann entitled: "Planning and Coding of Problems for an Electronic Computing Instrument." (Hereinafter referred to as Planning and Coding Report No. 1)

1 July 1947, by Bigelow, Hildebrandt, Pomerene, Snyder, Slutz, and Ware entitled: "Interim Progress Report on the Physical Realization of an Electronic Computing Instrument." (Hereafter referred to as Progress Report No. 2)

The present report on the physical realization of the computer is to be considered as a continuation of those listed above under the same title, and should be read in conjunction with them since many items referred to herein are discussed at some length in the previous reports.



It should be understood that the experimental techniques, component types, schemes for synthesis of primary organs, and design philosophy all are evolutionary and subject to revision as additional information emerges.

J.H.B.  
T.W.H.  
J.H.P.  
J.R.  
R.J.S.  
W.H.W.

#### N O T E

This report was written in fulfillment of contract obligations, at a time when the ideas of the experimental group were in a particularly formative stage, and when our limited technical staff was so overloaded as to be unable adequately to attend to questions of exposition. It was expected that the report would be given circulation limited to those personally in close touch with the progress of our group.

Many of the ideas set forth, and much of the apparatus described are out of date or superseded, and bear slight detailed resemblance to current practice of the group; and in some instances the description given of what was actually done or intended is inadequate to convey a clear integrated picture of the work to readers outside the intended circulation.

It is expected that a later, more complete report will be issued clarifying all of the questions concerning our current practices, as well as most of the points which remain of historical interest.

J. H. Bigelow,  
Chief, Engineer

May 26, 1950

## I. SUMMARY

The present objective of the development group is to produce at an early date what may be called a primitive, or laboratory, model of the computer (Model 0), which will be able to carry out computations but with control features of less than optimum convenience and with a less integrated design of the various organs. Then it is expected that the "final" model, Model 1, will be constructed on the basis of both the design experience and the mathematical experience obtained from the construction and operation of Model 0.

The planned computer is considered to consist of four primary organs: Input-Output, Memory, Arithmetic, and Control. For the input-output equipment, the Bureau of Standards is making equipment for preparing punched teletype tape from manuscript and for punching such tape from the data reproduced from a magnetic wire. The group at the Institute for Advanced Study is making equipment for recording from teletype tape to a magnetic wire, for mechanically handling the wire at high speed, for reading from the wire into the inner memory, and reading out from this memory onto the wire. With the exception of the last item, all of this equipment is now essentially in a form suitable for operation in the Model 0 machine. The last item has been considered in principle, and can be built as a relatively minor addendum to existing equipment. Work continues on the refinement of these items, and in particular on the construction of High-Speed Wire Drive No. 3, which is hoped to be suitable for the Model 1 machine as well as the Model 0.

The high-speed electronic memory equipment is being developed by the Radio Corporation of America, and is not discussed in this report.



The major progress has been in the realization of the arithmetic organs. The machine needs only two basic types of these organs: a shifting register of which two or possibly three will be used in the machine, and an adder (which includes subtraction) which will operate in conjunction with one of the shifting registers to form an accumulator. These have both been built in eight stages, and operated together satisfactorily under test conditions. As at present constructed, the minimum time in which a shift can be performed in the register is 2 microseconds. Tests made on the present eight stages indicate that for a complete 40-stage accumulator multiplication by the digit 1 together with a shift would take about 12 microseconds and a single addition without shift would take about 14 microseconds. It should be remembered that all of these figures are the least time in which the circuit will operate correctly, using optimum pulse widths and spacing. To provide for variations both in the accumulator and in the pulsers the actual time allowed for these operations may have to be appreciably greater than these figures.

In the control are included pulsers necessary to cycle the arithmetic organs in performing addition, subtraction, multiplication, and division and also the registers, counters, and gate circuits necessary to organize the individual components into a computer by sensing the successive orders of a problem and appropriately directing transfers and arithmetic operations. Work has been done on counters and pulsers, and a multiplication control has been constructed for a previous model of accumulator, but it should be said that in general work on the control is just starting intensively.

## II. INTRODUCTION

This report is intended as an extension of the previous reports that have been issued by this group under the same title. It describes progress that has been made during the last few months towards achieving the construction of a computing machine, rather than being a final report on a machine. As such, the description of progress is kept to a reasonable length by not repeating here the discussions and conclusions which have been presented in the previous reports. This report, then, should be read with close reference to the previous ones.

It will be remembered that the plans for the realization of an electronic computing machine entail the construction of a semi-experimental model of the machine called Model 0. This is to consist of an aggregate of equipment ---- including laboratory equipment ---- which will be capable of operating together in the solution of mathematical problems, but which does not have all of the automatic control features to be found later in the "complete" model, Model 1. Thus, for instance, it is expected that in the Model 0 machine the starting and stopping of the magnetic wire will be manually controlled: when the machine is in need of additional data from the magnetic wire, it will signal that fact by appropriate lights, and the operator will then have to direct the input equipment where on the magnetic wire to go for this data. For this reason in this model the data will be recorded on the magnetic wire in groups, with considerable blank wire between successive groups, and it will be required in the operation of this model that the whole group be read into the inner memory at once. This feature is required solely by the manual oper-

ation of the input mechanism, and is not expected to remain in the later model.

Physically it is expected that the Model O machine will consist largely of components built for testing in the laboratory, merely interconnected into a complete system. Thus for this model only relatively little attention is being given to problems of physical mounting of components.

It is anticipated that not only will the design experience gained from the construction of this preliminary model be useful in the later construction of the full machine, but also that during the time that the later model is in design and construction experience can be gained in the actual solution of problems on the model O, and that this experience may possibly indicate logical changes in the interconnection of the machine which will facilitate the mathematics of the operation. The Model O will undoubtedly operate at a somewhat lower speed than the Model 1, but the speeds should be sufficiently comparable to make the experience in operating the earlier useful in designing the later.

Of the major organs of the machine, this group is not at present concerned with any features of the inner high-speed memory. That is being developed by the Radio Corporation of America, and is not discussed in this report.

The electronic equipment for the input-output organs may be considered under several subdivisions:

- (1) the recording equipment which transcribes from the teletype tape to the magnetic wire;
- (2) the equipment which amplifies and selects the pulses read from the wire and indexes them for insertion in the Selectron memory;
- (3) the equipment which records the contents of the Selectron memory on the magnetic wire; and
- (4) the equipment which prepares a teletype tape from the information recorded on the wire.

Of these units, we have, as yet, no first model of equipment to transcribe from the Selectron memory to the wire, but there are models of other units in operating condition and under test.

#### 1. Input recording equipment

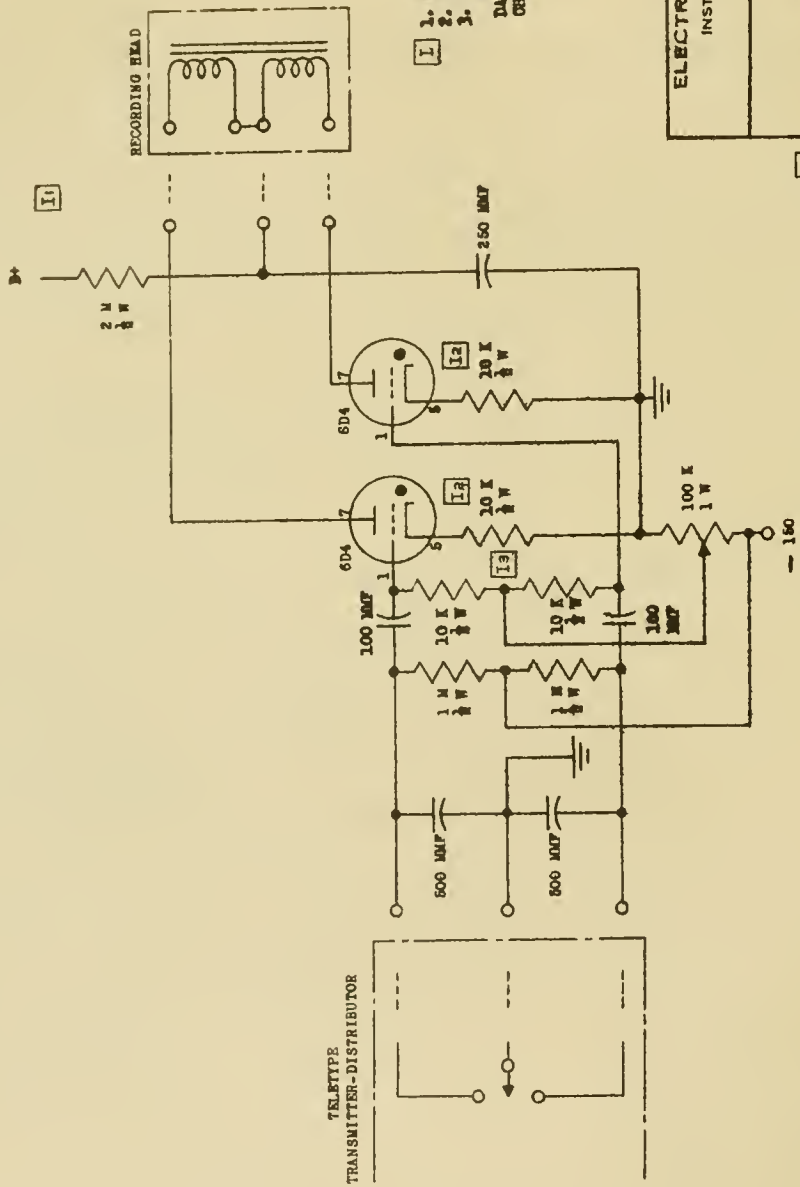
In order to obtain maximum space utilization on the wire when recording, it was found that pulses of very short duration were desirable, and the Recording Driver No. 2 was constructed to provide these pulses. (see Progress Report No. 2) It consists of two thyratrons, 6D4's, each connected to a separate half of the recording head, and triggered singly by the Teletype Transmitter-Distributor, depending on whether there is a punch or no-punch condition on the tape. As originally constructed, the grid of each thyatron was brought just to ground potential to fire the tube, but in the course of



subsequent work with the driver, it was found that the tubes occasionally fired more than once during the dwell of the transmitter-distributor brush on a single commutator segment. In order to eliminate this difficulty, and assure that the tubes always fired, the grid circuits of the driver were modified by the insertion of an additional short-time-constant filter. The resistance in the cathode circuits was also halved, in order to permit more current to flow through the recording coils. This brings the wire more nearly to saturation on each pulse, and, while it reduces the maximum pulse packing obtainable, it also reduces the variation of the peak voltage of pulses being read from the wire. See Drawing C-3-1009-I.

Erasing previously recorded information from the wire is a necessary preliminary to the recording operation. While the erasing operation is easily accomplished at low wire speeds, at the higher wire speeds it becomes a far more difficult problem. The chief cause for this difficulty is that as the wire speed is increased, the number of cycles per inch which can be recorded remains constant; thus frequency which produces erasure at low wire speeds is easily recorded on the wire at high wire speeds. Obviously, in order to obtain erasure, the frequency of the erasing signal must be correspondingly increased. This increase in frequency, however, introduces a secondary difficulty, that the impedance of the windings of the erasing head increases, and hence a large voltage must be established across the head to force sufficient current through it to saturate the wire.

There are at least two possible methods of approach in dealing with this erasing problem: the "brute force" method of providing the necessary current by



- ALTERATIONS**
1. 6D4 POT. DELAYED.
  2. CATHODE RESISTORS CHANGED.
  3. 100-mF CAPACITORS AND 10-K GRID RESISTORS INSERTED.
- DATA: 12-12-47 DRAWN BY: H.H.  
CHECKED BY: J.W.H.

ELECTRONIC COMPUTER PROJECT		INSTITUTE FOR ADVANCED STUDY		PRINCETON, N. J.	
RECORDING DRIVER NO. 2					
G - 1 - 1009 - I					
DATE	DRAWN BY	CHECKED BY	INITIAL		
7 - 17 - 47	H. H.	J.W.H.			

I4

- 180

use of powerful amplifiers, and the more refined method of redesigning the head used for erasing to make it especially suited to its task (we have been using for erasing a head identical to those used for recording on and reading from the wire, Brush type BK910).

A third method, which was actually attempted may be considered a modification of the first. The coils of the Brush recording head have a natural resonant frequency somewhere in the region of 100 kc. It was reasoned that with the head operating as a parallel resonant tank circuit in an oscillator, a high circulating current would be obtained with the expenditure of a relatively small amount of input power. Assembly of a head in a Hartley oscillator circuit showed that the losses were sufficiently low to permit successful operation as an oscillator. However, the frequency of oscillation (87 kc.) was still not sufficiently high to prevent some recording of the erasing signal on the wire at a wire speed of 157 in/sec. It thus appears likely that further work in this direction is necessary, probably involving redesign of the head for more satisfactory erasing properties.

In attempting redesign of a head for good erasing properties, an increase in the width of the gap in the head should be sought, as well as a reduction in the impedance of the head at the erasing frequency or an increase in the natural resonant frequency of the head, or possibly both. The increase in the gap width will insure that the wire is passed through more cycles at any given wire speed and erasing frequency. Reduction of the impedance by reducing the number of turns has the obvious consequence of reducing the voltage necessary to produce the same amount of flux in the magnetic circuit (since

the impedance depends on the square of the number of turns, and the flux depends linearly on the number of turns). Reduction of the number of turns will also have the effect of increasing the natural resonant frequency of the head.

At the present time the method of using the head as the tank circuit of an oscillator to obtain the erasing signal is being used satisfactorily at relatively low wire speeds, up to about two feet a second. For more satisfactory operation, the frequency of the oscillation has been reduced to about 34.5 kc. by the addition of capacitance in parallel with the distributed capacitance of the head. See Drawing C3-1023; and Photograph 1.

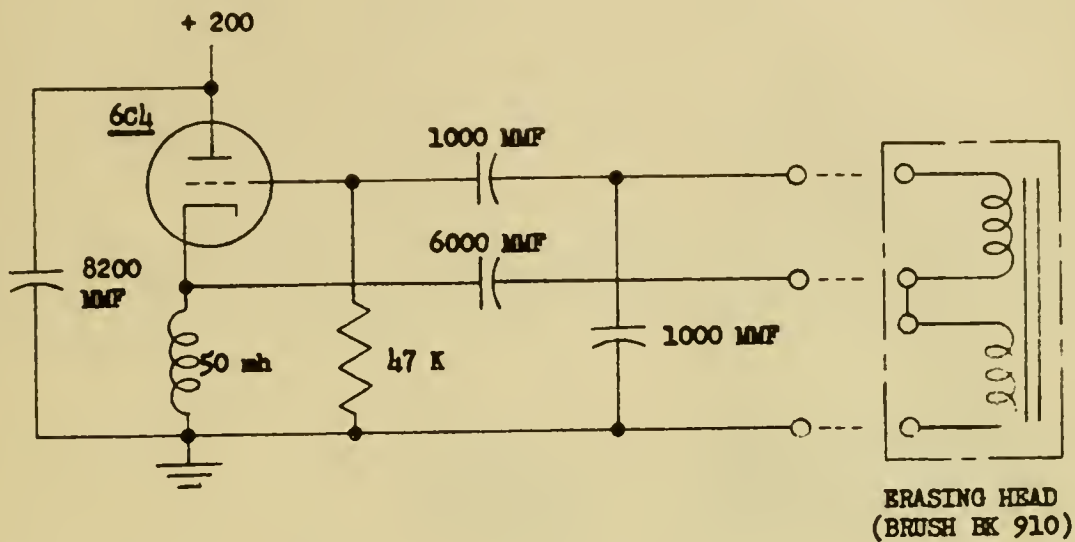
## 2. Input Distributor Rack

The units of the input distributor, the electronic section which receives information from the wire and checks it, deleting the coding pulses, preparatory to placing the information in a register for insertion in the Selectron memory, have been assembled on a single rack for convenience of operation (see Progress Report No. 2). These units include the amplifier (General Radio Type 714), the pulse limiter, the pulse shaper, and the pulse selector, these last three reassembled on a single chassis; the input distributor, chassis 1 and 2; and associated voltage dividers and regulators.

Photographs 2a and 2b show the new limiter, shaper, and selector chassis. This chassis constitutes an experiment in mechanical layout with a view toward providing ready access to all components for repair work, and to providing for the ventilation of the components.

Certain minor modifications were made in these units to make their operation more reliable. In the pulse selector, a small amount of delay was





# ELECTRONIC COMPUTER PROJECT

INSTITUTE FOR ADVANCED STUDY

PRINCETON, N. J.

ERASING OSCILLATOR

C - 3 - 1023

DATE

12 - 5 - 47

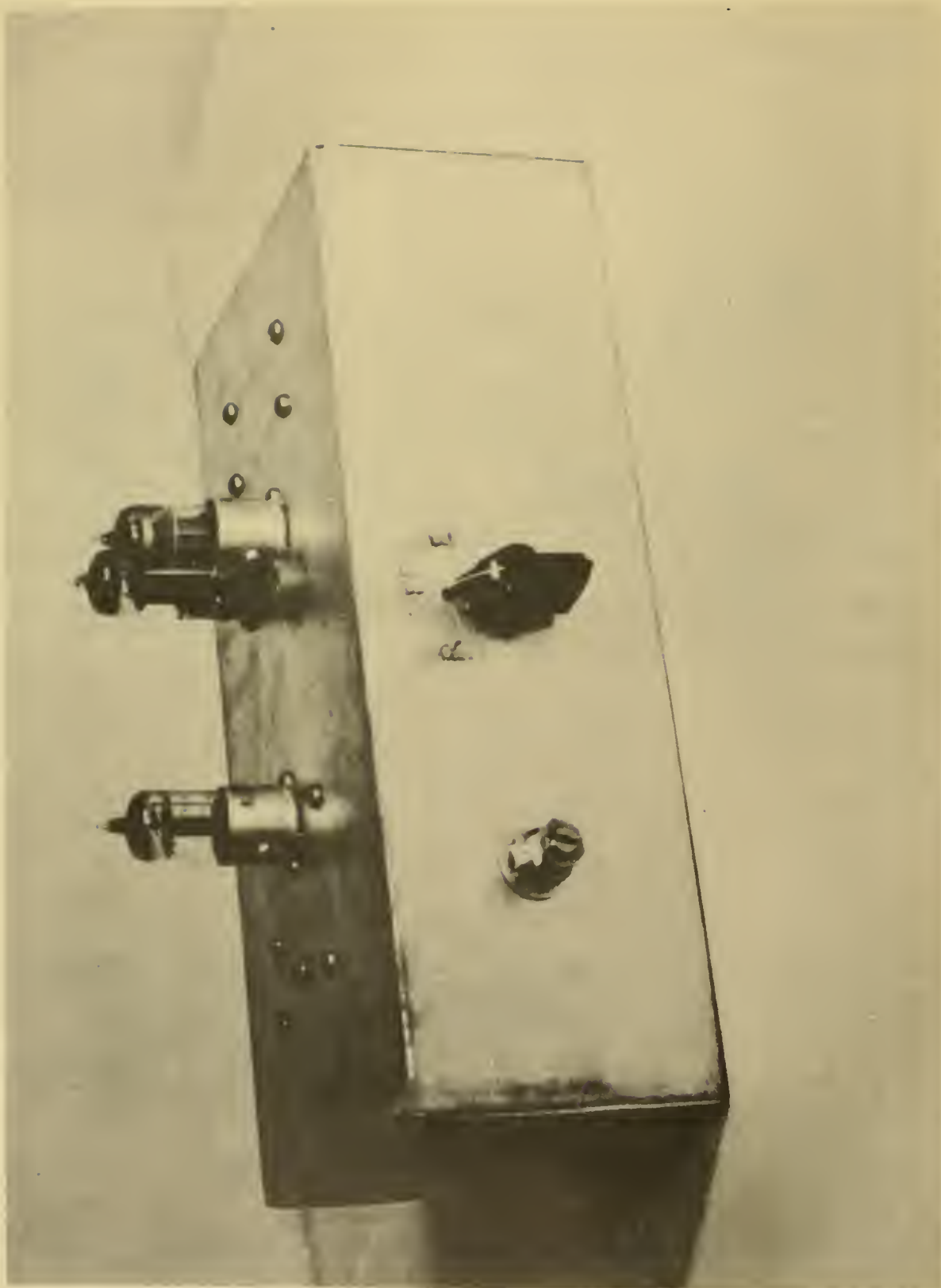
DRAWN BY

H. HART

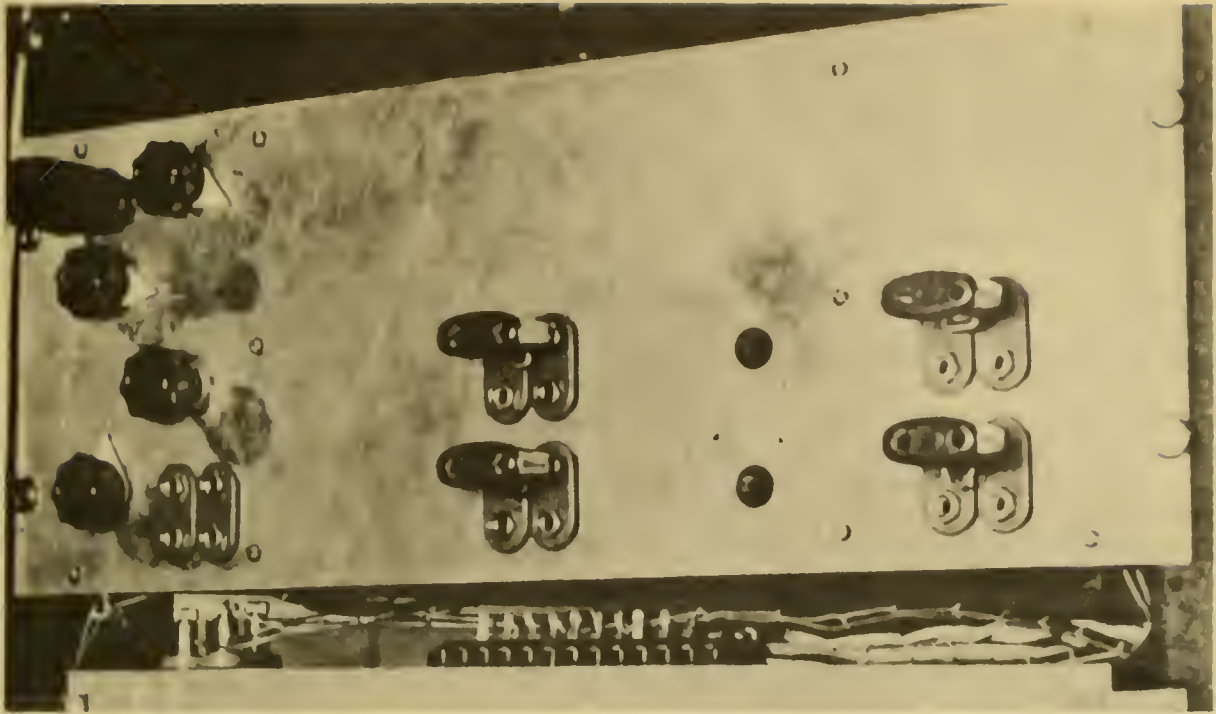
CHECKED BY

*THA*

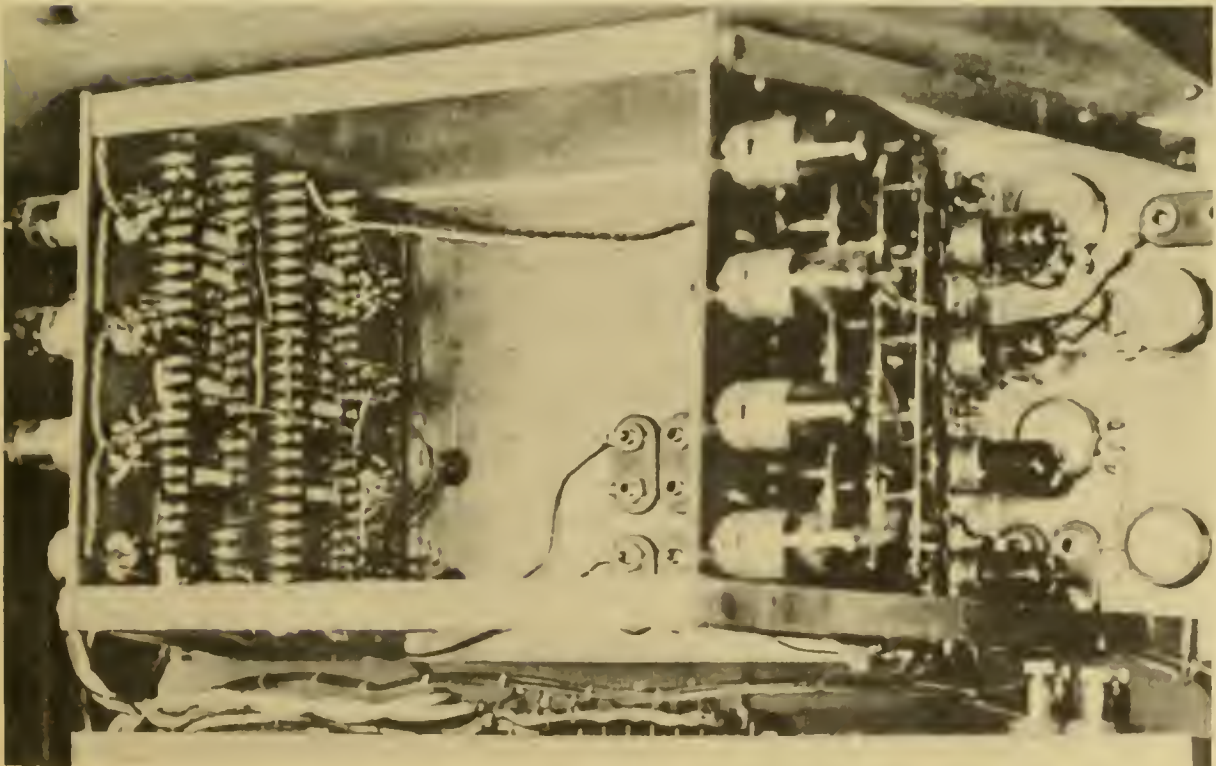
INITIAL



Photograph 1. Erasing oscillator and recording driver.



Photograph 2a. Limiter, shaper, and selector chassis. Front view.



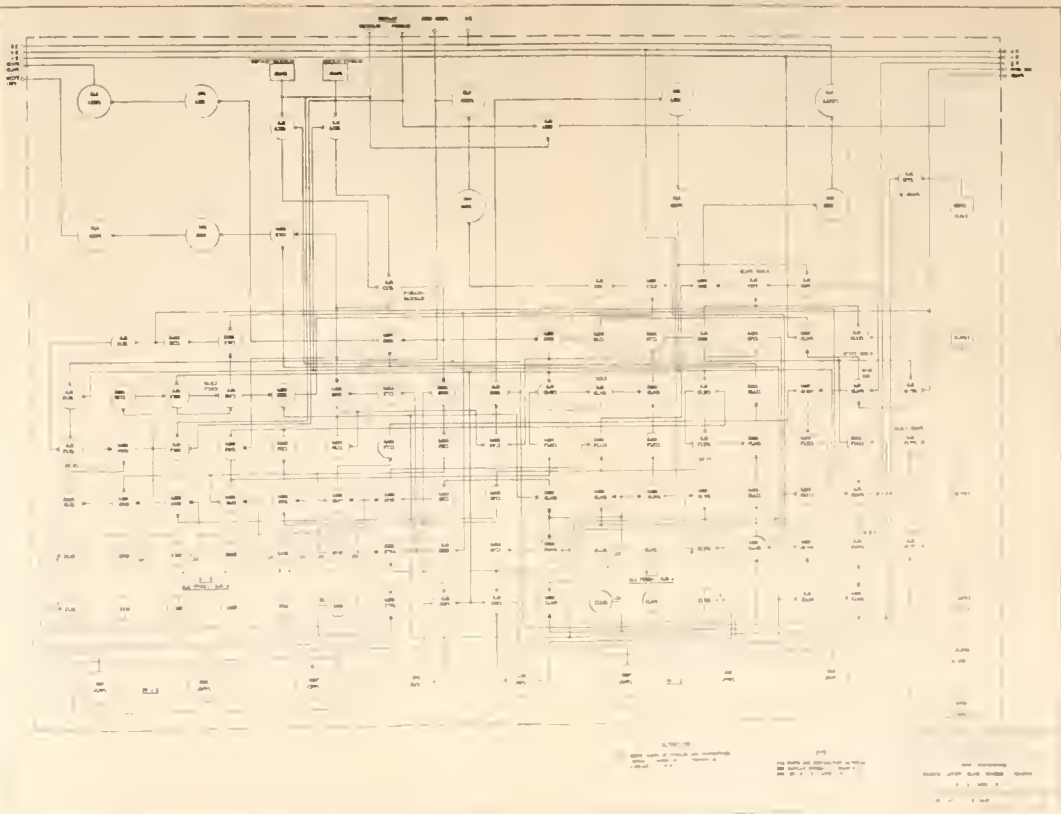
Photograph 2b. Limiter, shaper, and selector chassis. Rear view.

added to the selecting gates, to make sure that they remained open until the desired pulse of a pair had passed through. The delay consisted of a shunt capacitance of 5.6 mmf. placed between the gate grid and ground.

Other minor modifications were made in the second chassis of the indexer. The only change in its logic dealt with the OK-error toggle, which formerly, when the wire was being run backward, was set (neon on) on any word-end pulse occurring on a pulse whose number is divisible by five, except the 55th pulse; after the modification, the toggle was placed in the set condition by any word-end pulse, except one occurring on a pulse numbered 51 through 55. Thus in the absence of a word-end, the 56th pulse supplies a "simulated" word-end pulse occurring on the 56th pulse and sets the OK-error toggle. One other modification was made to slow up a gate, so that the desired pulse would be transmitted before the gate closed.

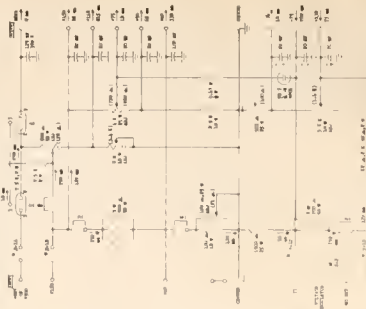
The diagram, Drawings C-3-1002-D, and C-3-1002-G may require a word of explanation. C-3-1002-D shows the location of the tubes on the chassis, and shows only the flow of the signals through the unit. Since there are in the unit only relatively few basic circuits, each of which is repeated several times in different locations, Drawing C-3-1002-G shows only these basic circuits and provides a wiring table which shows the interconnections of these basic circuits in the chassis. This method of showing a large and logically complicated unit is considered to be more economical and otherwise more satisfactory than to use a complete overall circuit diagram.

In assembling these units on a single rack, it was necessary to provide voltage dividers to supply all the voltages for the operation. The divider

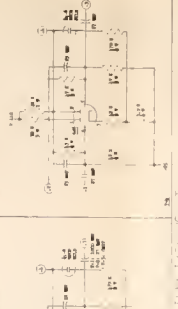




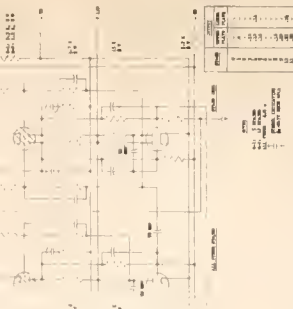
# CALCULATOR



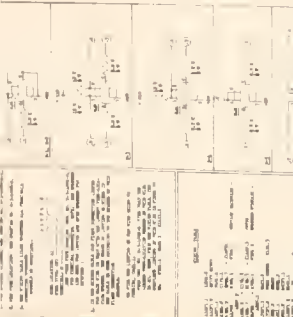
1. The calculator is designed to perform mathematical operations on the data provided by the input unit. It is capable of performing addition, subtraction, multiplication, and division. The calculator is also capable of performing more complex operations, such as squaring and square root. The calculator is designed to be accurate and reliable, and it is capable of performing operations on a wide range of numbers.



2. The calculator is designed to be accurate and reliable, and it is capable of performing operations on a wide range of numbers. It is also capable of performing more complex operations, such as squaring and square root. The calculator is designed to be easy to use and to provide accurate input to the calculator.



3. The calculator is designed to be easy to use and to provide accurate input to the calculator. It is also capable of performing more complex operations, such as squaring and square root. The calculator is designed to be accurate and reliable, and it is capable of performing operations on a wide range of numbers.



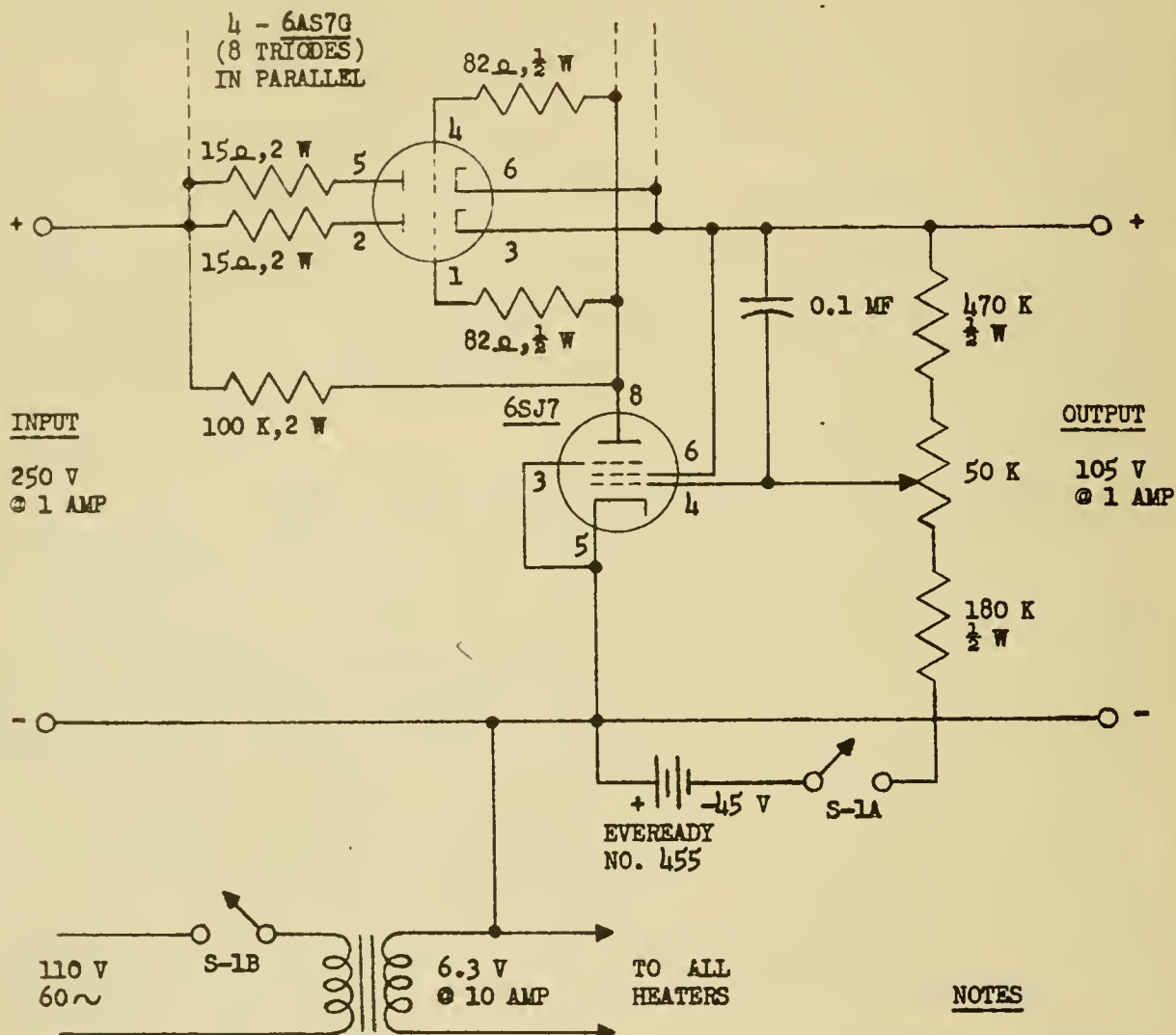
4. The calculator is designed to be accurate and reliable, and it is capable of performing operations on a wide range of numbers. It is also capable of performing more complex operations, such as squaring and square root. The calculator is designed to be easy to use and to provide accurate input to the calculator.

for chassis II of the indexer is shown also in C-3-1002-G. This divider is designed so that it can be adapted to various combinations of d-c power supply.

Certain of the voltages for the operation of Chassis II were obtained from a motor-generator set. When trouble was experienced from voltage variations at the output of the motor-generator, a voltage regulator (C-2-1026) was installed. The regulator, besides providing a constant d-c voltage as required, also served in lieu of an L-C filter to remove commutator ripple and hash from the output of the generator.

### 3. Equipment for transcribing from inner memory to wire.

As mentioned above, no equipment for this function is yet constructed. However, a possible method of obtaining the necessary pulses in the proper sequence is shown in Drawing C-3-1032. This consists essentially of a five-stage ring and an eleven-stage chain together with several gates. This provides the following desired pulses: The first pulse from the 25 kc clock is recorded as a minus pulse on the wire; the next four pulses from the clock record plus or minus pulses, followed by a shift of the register, depending on which of the two gates associated with the register is open. This cycle is repeated for each group of five clock pulses up to the beginning of the eleventh group. At this point another gate is opened which records a group of five plus pulses, the word-end signal. When this sequence has been completed, a pulse goes to the off-on toggle shutting this circuit off until a new word has been recorded in the register from the Selectron memory. The control will then supply a new start pulse and the sequence of 55 pulses will be repeated. It should be noted that this plan only takes into account that the wire may be moving forward



#### NOTES

1. NO CHASSIS GROUNDS.
2. S-1A AND S-1B CONSTITUTE A DOUBLE-POLE, SINGLE-THROW SWITCH.

### ELECTRONIC COMPUTER PROJECT

INSTITUTE FOR ADVANCED STUDY

PRINCETON, N. J.

ONE - AMPERE VOLTAGE REGULATOR

C - 2 - 1026

DATE

10-13-47

DRAWN BY

H.H.

CHECKED BY

JWH

INITIAL



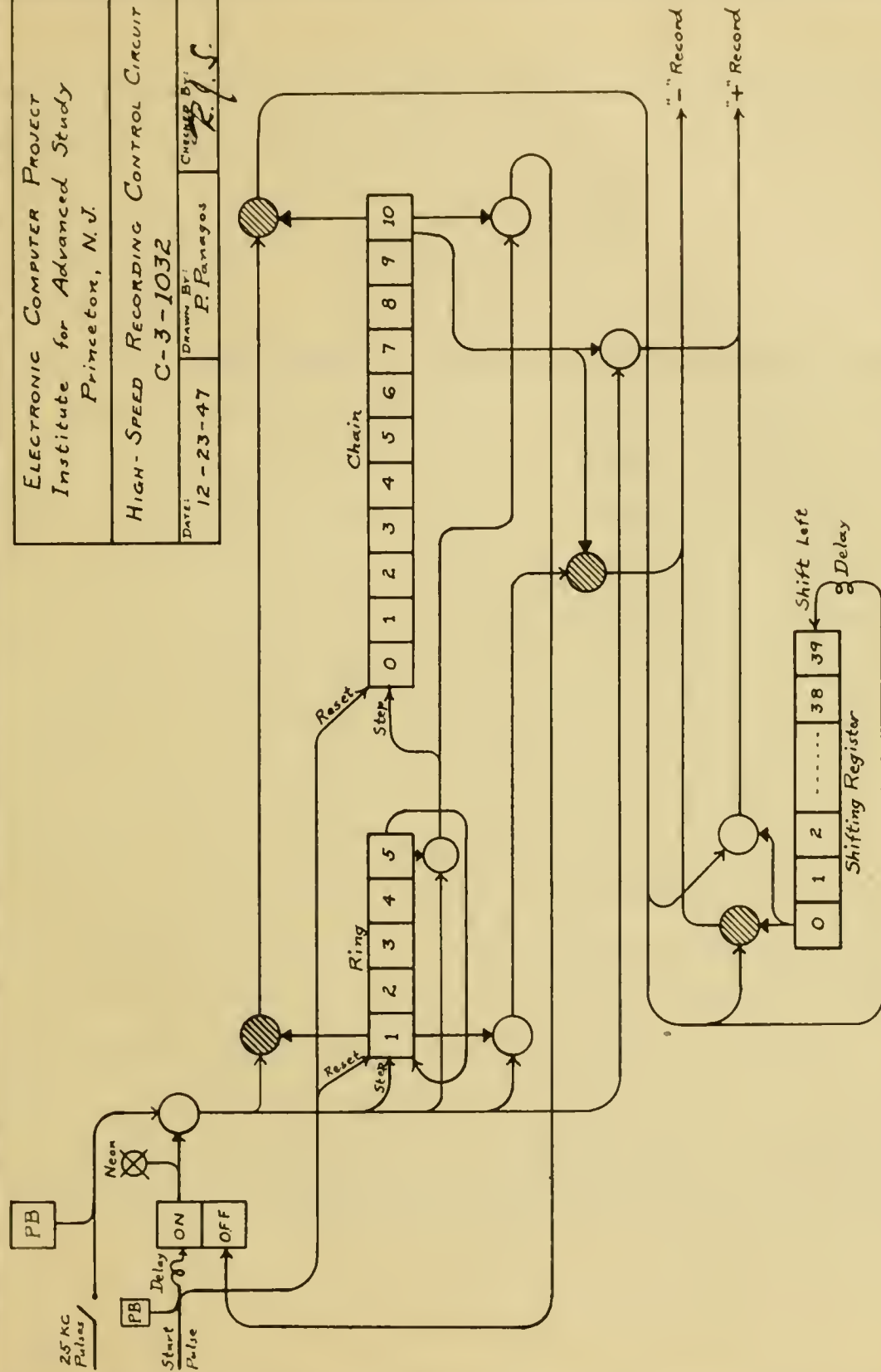
ELECTRONIC COMPUTER PROJECT  
Institute for Advanced Study  
Princeton, N.J.

HIGH-SPEED RECORDING CONTROL CIRCUIT  
C-3-1032

Date: 12-23-47

Drawn By: F. Panagos

Checked By: R. J. S.



during the recording operation. This is in line with the plans for the Mod. O machine.

It is also interesting to observe in this connection, that two of the essential elements of this circuit are already in existence in the Indexer chassis II, the five-stage ring and the eleven-stage chain. Thus it may be possible to obtain the recording function by using a comparatively simple "addendum" with the existing indexer equipment.

#### 4. Equipment for transcribing from wire to teletype tape.

This section of the output equipment has been under development in the Ordnance Division of the Bureau of Standards. At the present time the development is essentially complete and we are awaiting the shipment of this equipment (together with other units developed at the Bureau) to Princeton. There is considerable basic similarity between the elements of this unit and the Input Distributor mentioned above --- both operate on pulses reproduced from the magnetic wire --- but there is considerable difference in the organizational logic of the two circuits. While the Input Distributor handles pulses going from the magnetic wire into the Selectron memory, this unit handles pulses going from the magnetic wire into a punched teletype tape, which calls for different handling of the pulses. Thus the unit contains an amplifier, a pulse shaping and selecting circuit, and an indexer which checks for the presence of the coding pulses in their proper sequence, but once synchronism is obtained, the output is fed alternately into two five-stage registers, which, in turn, are "dumped" into a mechanical tape punch. The use of the intermediate step of punching a paper tape rather than directly printing the information is for

the purpose of speeding up the operation ; the punch is capable of operating three times as fast as the printing circuits, and so by its use it is possible to transcribe more information through a single channel, although it requires the handling of the paper tapes .

## B. MECHANICAL EQUIPMENT

### 1. Teletype equipment

Word received from the Bureau of Standards recently indicates that the modified teletype units of the input-output equipment are finished except for a few minor features. These units include a Typing Reperforator with modifications in the keyboard and printed characters; a tape comparator and proof-reader, which is a modified Model 19 Perforator Transmitter and Page Printer, with which the corrected paper tape is prepared by comparing it with the first tape, and a page copy of the tape is prepared simultaneously; a modified Transmitter Distributor for recording from the teletype tape to the magnetic wire; the punch to be used in conjunction with the electronic equipment for preparing a teletype tape from information recorded on the wire; and auxiliary devices, such as tape reels and rewinding equipment. This equipment has been seen in operation by representatives of the Institute and found to be essentially well suited to our requirements. It is expected that the equipment will be delivered from the Bureau of Standards within a very few weeks.

### 2. High-speed wire drive

a. Drive No. 2 In connection with the low-speed and high-speed wire tests (see below) the High Speed Wire Drive No. 2 was utilized. While this plate

model was not intended to be used as a piece of laboratory equipment, since it did have several obvious limitations, it was felt that some time would be saved by making use of it in the laboratory. Accordingly, it was fitted with a gear combination and another Delco permanent magnet, geared motor to provide a low speed drive for recording and reading at low speeds, in addition to the usual 1/2 hp. three phase motor for high-speed operation.

This method of low-speed drive was not found to be satisfactory for test purposes, since variations in the speed of the motor produced varying spacing in the recorded pulses during the recording process, and commutator hash from the small d.c. motor completely obliterated the signal from the wire during attempts to read from the wire at low speed. Hence, a small "Ratiomotor", a geared induction motor, was obtained and coupled to the high-speed motor by a belt, the latter motor then serving as a countershaft. This eliminated the effect of speed variation to a large extent, and made it possible to view the output from the wire conveniently on an oscilloscope.

However, a new interference problem was then discovered. The servo-motors which turn the reels with respect to each other to regulate the loop length (see Progress Report No. 2) are also of the permanent magnet type, and are operated by switches which are, in turn operated by the arm carrying the loop takeup idler pulley. It was found that arcing in the switches produced interference pulses every time the servo action took place, and that these pulses were about the same amplitude as the information pulses being read from the wire when the wire was operated at a speed of about two feet per second. Attempts to eliminate the interfering pulses included capacitive filtering and

thorough shielding, and, while their amplitude was reduced slightly, they were by no means eliminated.

Work toward the elimination of this interference so that successful tests at low speed can be made with a long wire is still in progress. The eventual solution may take one of several forms. It may be that the use of a vacuum-tube relay with heavy filtering at the operating switches will provide the answer. Failing in all attempts to retain the servoing feature while eliminating the interference from it, we may finally eliminate the servoing system altogether, and build a separate drive mechanism for operation at low speeds, which will be capable of using the same reels as the high-speed drive.

It should be emphasized that the difficulties referred to in these paragraphs were found only in using the high-speed drive for low-speed operation --- a use which was not included in its design.



b. Drive No. 3 As indicated in earlier progress reports (PR 1 and 2) high-speed wire drives pos. 1 and 2 were experimental; no. 1 having been built from whatever was at hand to demonstrate the feasibility of the idea, and no. 2 being a "plate model" to study the behavior of the arrangement when reduced to something like final size, and was deliberately designed with a direct-current on-off servo-system to permit study of the performance at various speeds and operation conditions. Use of this plate model in experimental work involving the characteristics of the recording head and amplifying system was purely incidental, and, in particular, the use of the plate model in low speed reading and recording tests was purely opportunistic.

Drive No. 3 represents the first attempt to embody these ideas and experiences into a component somewhat like a final form. As discussed (in PR 2) drive No. 3 has a fully enclosed coaxial servo system with a small 3-phase motor built directly into the main drive shaft, and the servo excitation is proportional to loop periphery rather than in "on-off" relationship to loop deviation. The proportional relationship is accomplished by means of a miniature selsyn transformer coupled to a light follow-up system having a pair of balanced and symmetrical arms establishing the loop size and tension. (See Fig. 3E.) These follow-up arms are terminated by pulleys each completely enclosing a pair of miniature Swiss ball bearings running in oil; and the arms are pivoted on similar bearings to the frame of the traverse system, which itself is suspended from preloaded ball bearing pivots to the main mounting plate. This entire arrangement carries the magnetic recording heads and is to traverse back and forth slowly to provide level-winding. The arrangement is fully encased in a small cabinet having a window in the bottom, through a mirror arrangement will permit inspection of the head and follow-up system.

Except for the gear train and cam providing traverse motion, this outfit has been entirely built and appears to operate well. The power auxiliaries include a 3-phase 400 cycle attenuator devised from three single-phase units, together with D.C. excitation, suitable transformers, meters, and switches. (See Fig. 3F.) This power unit will be adequate to operate any number of high speed wire drive units via a central exchange switching system.

Wire drive No. 3 uses the same reel size as tested and found satisfactory in the plate-model (No. 2) and the reels are permanently coupled in pairs (Fig. 3A) and are arranged to be quickly demountable by means of a torsionally rigid and slack-free coupling (Figs. 3B and 3C) permitting instant removal regardless of the status of the winding process. Upon removal of the reels from their mount (see Fig. 3E) the entire traverse frame and mechanism can be swung outward and up for inspection.

At the drive-end of the differential servo housing a fully enclosed electrically retracted brake has been built into the enclosure formed by the drive pulley, and a small direct-coupled D.C. magneto tachometer provided to permit verification of rotation direction and speed by feed-back into the control system so that in case of relay failure, belt breakage, motor or other mechanical failure such fact is reported to the central control independently of reaction via the channel of command.

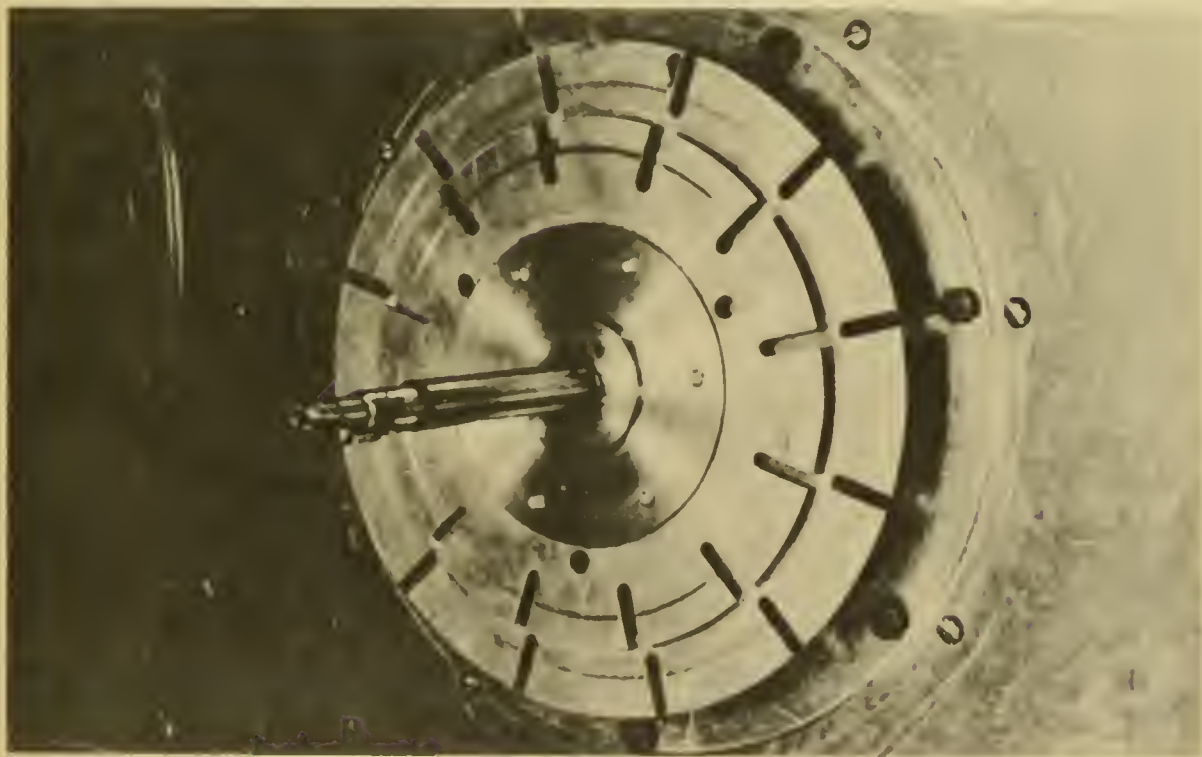
The traverse system cam and gear train, together with the door upon which they mount have been entirely designed and are in process of construction. No difficulty is anticipated in this part of the system, and as soon as the unit is complete it will be thoroughly tested and at least two additional replicas made. To date the design has proven so satisfactory that

only minor changes are anticipated between the present model and the replicas -- primarily, certain tolerances will be relieved to facilitate assembly and manufacture. Beyond this, it is expected to add emergency switches to the follow-up system to cut power and apply the brake in case of any accident such as wire breakage, etc. Also an idea has been evolved for appending a slow-speed drive attachment suitable for operation at teletype speeds; this will be designed and developed when time permits, and may permit fully automatic remote operation of the wire drive system obviating the chief necessity for removing and manipulating wire reels.

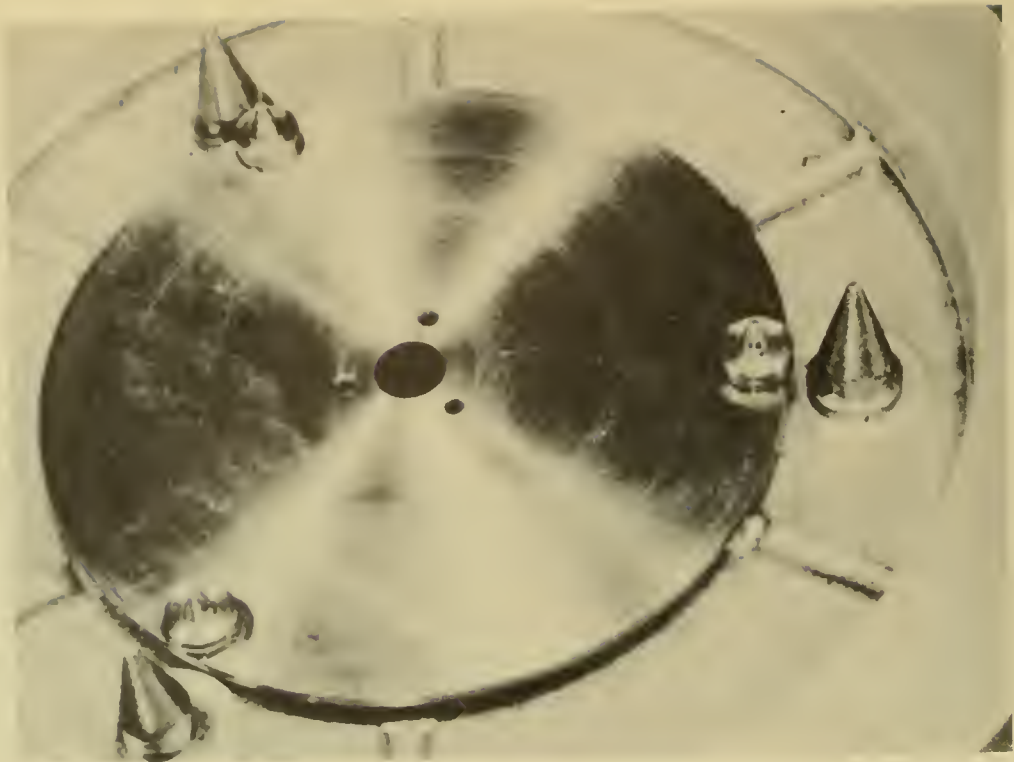




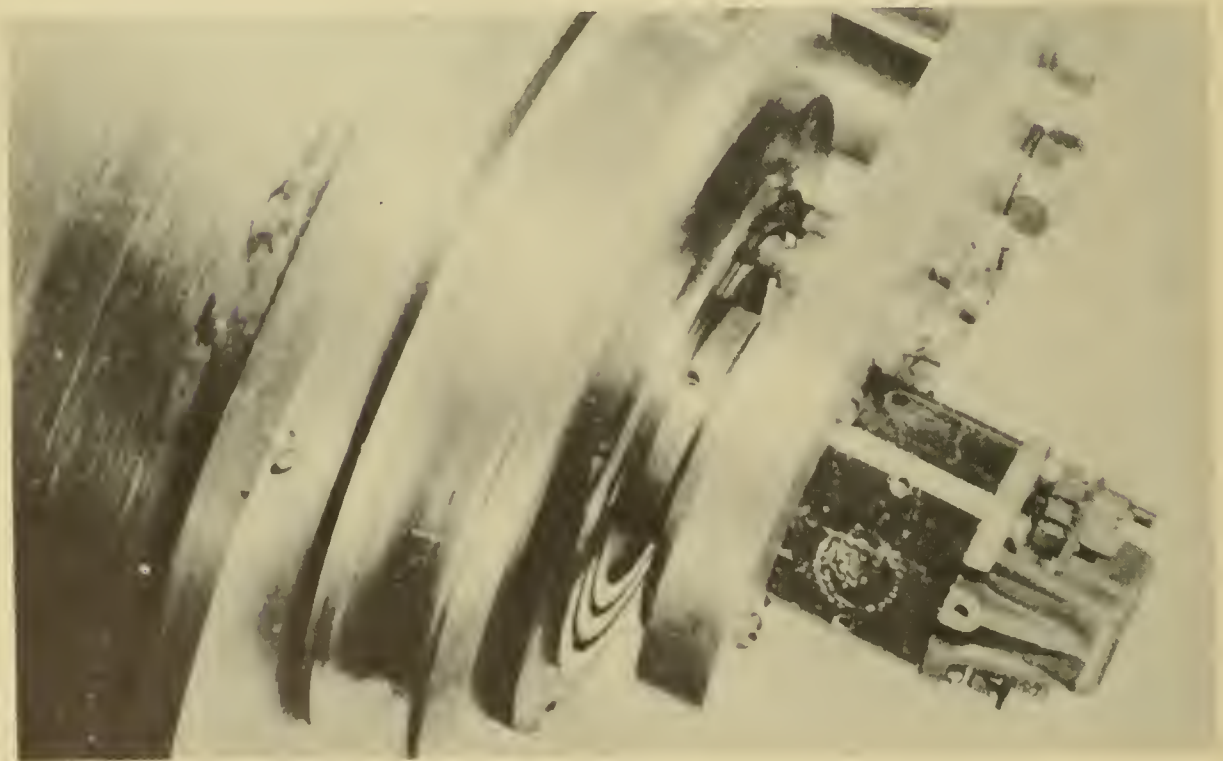
Photograph 3a. High speed wire drive No. 3; wire reels in place.



Photograph 3b. High speed wire drive No. 3; index mechanism for wire reels.



Photograph 3c. High speed wire drive No. 3; index pins of wire reels.



Photograph 3d. High speed wire drive No. 3; tachometer, drive pulley, and slip rings.

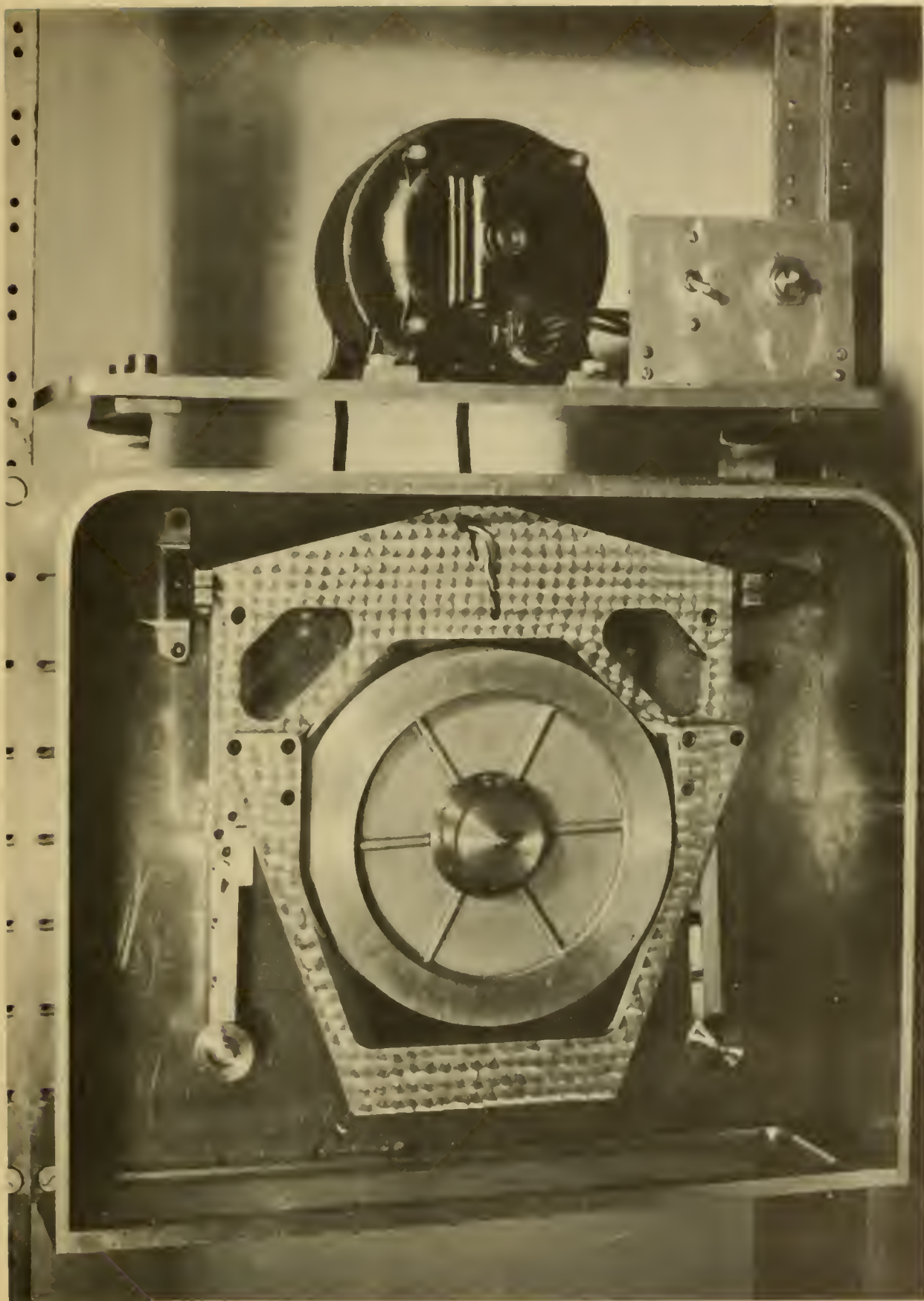


Figure 3E. High speed wire drive No. 3; assembly showing traverse system.



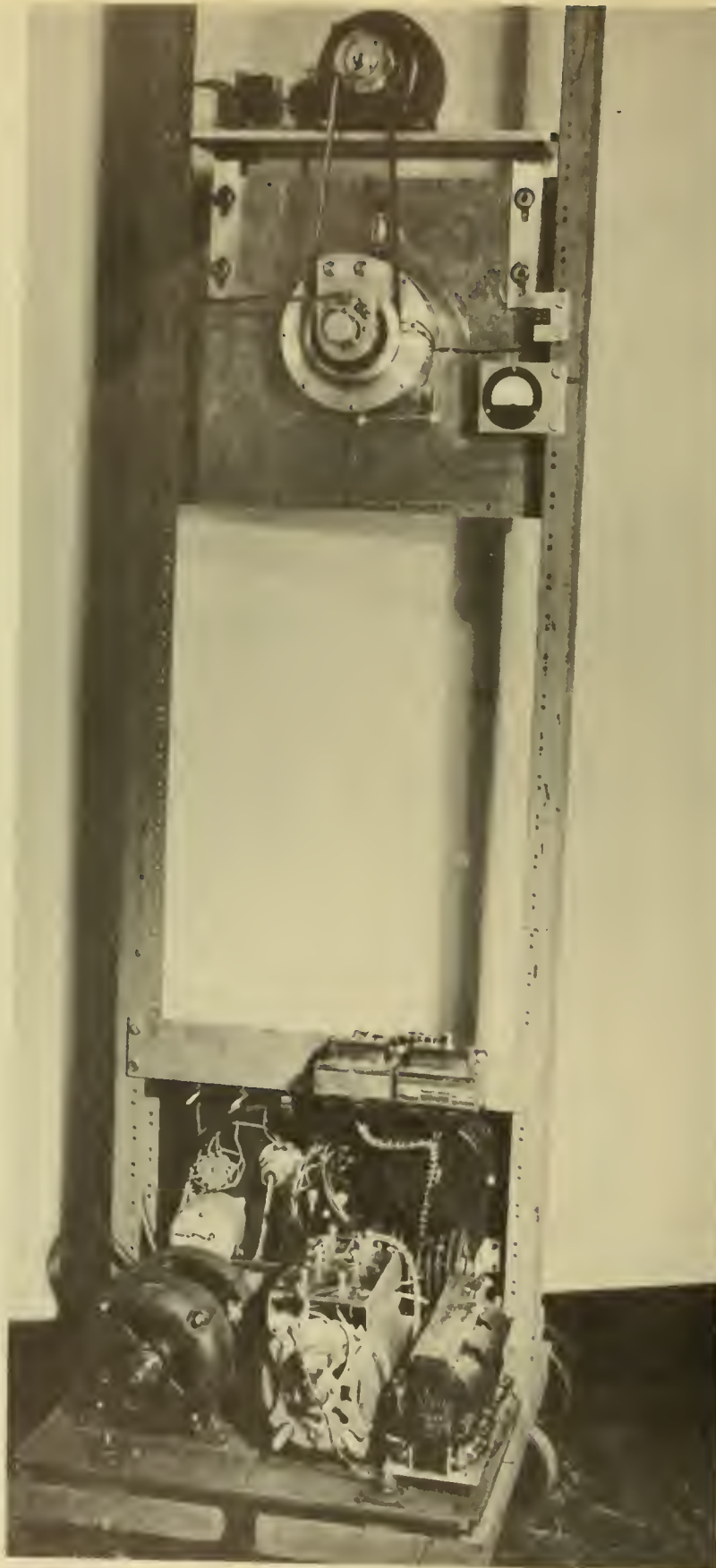


Figure 3F. High speed wire drive No. 3. (Assembly showing Drive and Power Auxiliaries)

## C. RECORD-REPRODUCE TESTS

### 1. New Brush wire

Following the decision that Brush type BK 913 plated brass magnetic recording wire was the most suitable wire obtainable at the moment for use in the computer, an order was placed with the Brush Development Company for 100,000 feet of that type of wire. Upon receipt of the shipment, it was discovered that a new type of Brush wire had been shipped, designated type BK942. Upon inquiry it was learned that the new wire was identical in its magnetic properties to type BK 913, but that it had superior mechanical properties, due to the use of Everdur (an alloy of copper, silicon and manganese) as the base metal instead of brass. Subsequent tests substantiated the claims of the manufacturer. The improved mechanical properties of the new wire make it especially resistant to kinking and subsequent breakage, and hence more easily handled.

### 2. Tests with loop drive

Following push-button tests of the equipment which had been assembled in the rack, tests were made using words recorded on a loop of wire operated in the Low Speed Loop Comparator (See Progress Report No. 2). As a result of these tests, and before successful operation of the complete indexer system could be achieved, the modifications mentioned above in Section IIIA were made to the input recording equipment and the input distributor rack.

Following these modifications, it was found that completely satisfactory operation of the indexer was possible when the recorded information was read from the wire at speeds as low as  $7/8$  inch per second, the recording speed, and as high as the maximum speed of the Loop Drive, 21 inches per second.

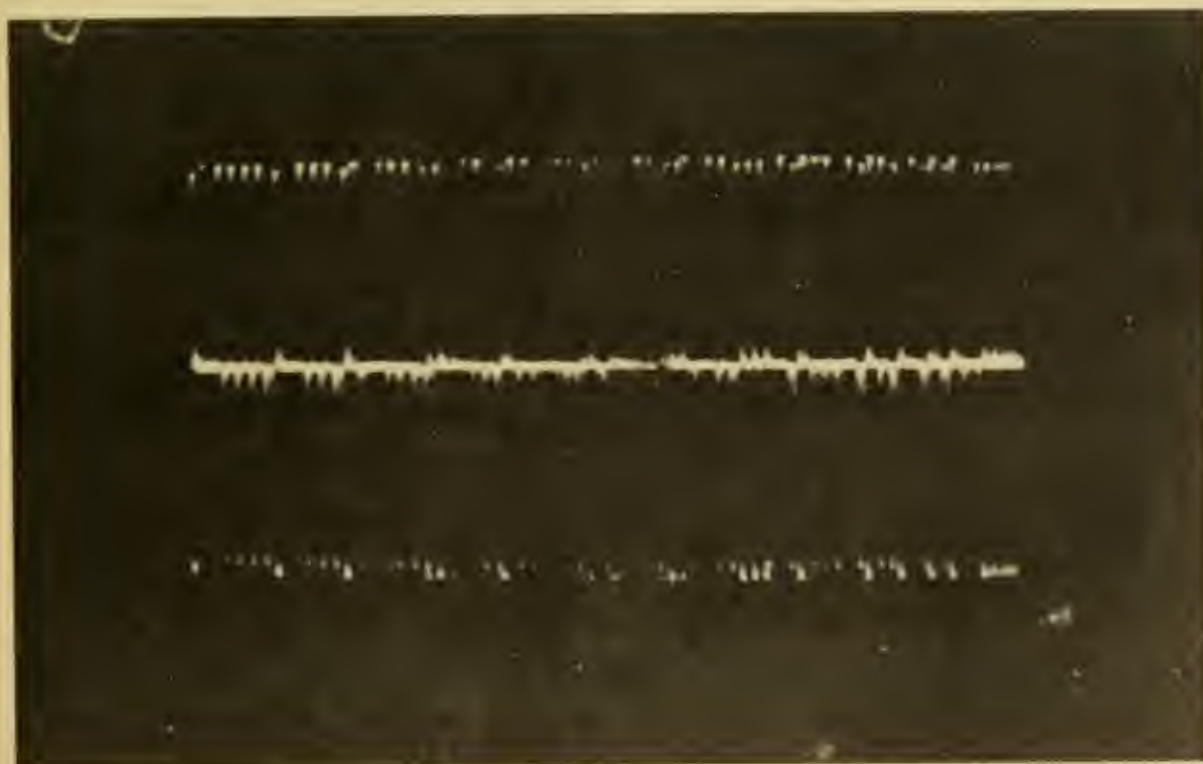
Only one further precaution needed to be observed in order to have perfect operation over many circuits of the loop: it was necessary to take care that the joint of the loop was not exposed either to the demagnetizing signal or to the recording pulse signal. For if the joint of the loop was exposed to any magnetizing signal when passing through the head, it was certain to produce an unwanted pulse during the reading out process. This unwanted pulse, naturally, caused the first word following the joint to be read incorrectly, even though the equipment was otherwise operating correctly.

As a result of this observation as to the effect of joints in the wire, it is likely that in the first models of the machine we shall require that there be no joints whatsoever in the wire, and that any wire which becomes broken will be used only to get the information out of it which is already recorded, and will then be discarded.

Using the loop to provide the input signal for the input distributor rack permitted the observation on an oscilloscope of the pulses in the system. If the information was recorded at  $7/8$  inch per second and read off the wire at ten or twenty inches per second, it was possible, by synchronizing the oscilloscope with the word-end pulse, to observe a complete word at one time. This is shown in Photographs 4a and 4b. 4a shows the word as it came out of the amplifier, without any limiting or shaping, while Photograph 4b shows the word after it has passed through the limiter which removes small variations near the axis and also limits the maximum amplitude. In the first picture the sign of the recorded data pulses may be read by observing the sequence of successive pulses, and remembering that a single positive recorded pulse is reproduced as a



Photograph 4a. Oscillogram of word reproduced directly from magnetic wire.



Photograph 4b. Oscillogram of word after limiting.



positive-negative pair, while a negative recorded pulse is reproduced as a negative-positive pair. In the second picture the sign of the original data pulses are even easier to read because a slight assymetry in the limiter results in different amplitudes for the two different pulses. The word recorded was 1,2,3,4,5,6,7,8,9,10, word-end. It will be remembered that each of these numbers is expressed in its binary form and that each group of four pulses is preceded by a negative marker, except for the 11-th group which, being the word-end group, consists of five positive pulses. The 55 pulses shown in the oscillograms are not quite evenly spaced, but are broken into groups of five pulses each. This is because mechanical reasons dictated that the recording commutator should not have its five active segments quite uniformly spaced; a slightly larger space is left in one location to provide for the advancing of the paper tape.

### 3. Tests with the high-speed drive

As mentioned above, there were several modifications found necessary on the high-speed drive, the plate model or Wire Drive No. 2, before it was possible to obtain satisfactory operation using it. Although not all of the necessary modifications and improvements have as yet been completed, some interesting data were obtained after providing the drive with a more satisfactory low-speed motor permitting reasonably evenly spaced recorded pulses during recording from the teletype (at low speeds, the operation of the servo motor causes a slight variation in the spacing of the pulses, but it has not proved to be a serious difficulty). The lowest speed obtainable with this new low-speed drive motor and the pulleys presently available is about  $1\frac{1}{2}$  inches



per second, and the wire was recorded from the teletype at this speed.

While, because of the interference from the servo system, it was not possible to read information successfully from the wire at low wire speeds, at speeds of  $13\frac{1}{2}$  or  $22\frac{1}{2}$  feet per second it was possible to read out successfully the information on the wire. The latter speed is the maximum considered safe with this drive.

Although there is every reason to believe that we have not reached the high-speed limit of successful operation, if we assume that the limit has been reached, we may make some interesting calculations. The teletype reads information from the punched tape onto the wire at the rate of about two seconds per word. Assuming that the inner memory will have a capacity of four thousand words, it would take eight thousand seconds, or more than two hours to read the contents of one memory onto the wire. We have demonstrated above that it is possible to record information on the wire at a wire speed of  $7/8$  inch per second (it is, in fact, possible to record satisfactorily at one-half this speed), and to read it out at the rate of  $22\frac{1}{2}$  feet per second, a ratio of about 300 to 1. Thus, at  $22\frac{1}{2}$  feet per second, we can fill the entire four thousand word inner memory in less than half a minute. Increasing the ratio of the maximum to the minimum wire speed will result in a corresponding decrease in the time necessary to fill the inner memory from the wire, and we fully expect to make the ratio several times as large.

#### D. ADDITIONAL MARKER PULSES

When a single pulse is recorded on magnetic wire, its reproduction consists of a pair of pulses of opposite sign. The polarity of the recorded pulse is indicated by the sequence of the pair; thus a positive recorded pulse will produce, say, output pulses which consist of a positive followed by a negative, while under the same conditions the recording of a negative pulse would reproduce as a negative pulse followed by a positive one. As has been discussed in the previous progress reports, there are a number of ways of eliminating the unwanted pulse; we have experimented with processes involving integration of the output voltage, differentiation of the output voltage either once or more than once, and counting and gating techniques to select the desired pulse and delete the undesired one. At the present time we are using the last method. The circuit of this Pulse Selector was described in the previous report. It operated basically by deleting every second pulse, but this is in itself insufficient: every time that the wire is started it is necessary to get the circuit in synchronism with the pulses for otherwise it would delete the wanted pulse and pass the unwanted one, making nonsense out of the data. As long as the recorded pulses are all of the same sign there is no distinguishing feature which the circuit could use to determine this synchronism. The reproduced signal then consists of a sequence of alternating positive and negative pulses, and there is no technique based solely on counting and a knowledge of the sign of the pulses which could possibly tell how these alternating pulses should be paired --- whether a pair should consist of a positive followed by a negative or whether it should be a negative followed by a positive. When the

sign of the recorded pulses changes, however, it is possible to determine the proper pairing of the pulses. Suppose, for example that the recorded sequence were + + - -. Then the reproduced sequence would be + - + - - + - +. If on the other hand, the recorded sequence were - - + + the reproduced sequence would be - + - + + - + -. Notice that where the sign of the recorded pulse changes, there appear in the reproduced pulses two adjacent pulses of the same sign; accordingly whenever two adjacent pulses of the same sign appear in the reproduced signal we know that the former is the second pulse of the previous pair and the latter is the first pulse of the next succeeding pair. The Pulse Selector includes a synchronizing circuit which works on this principle, re-synchronizing the counter whenever two adjacent pulses of the same sign are received.

The importance of this feature to the operation of the Indexer is that when the magnetic wire is started up in the middle of a word it may continue for several pulses with the Pulse Selector out of synchronism until a change of the sign of the recorded pulse appears and synchronizes it. If, for instance, the particular word being read were to have all of its data pulses negative then the negative marker pulses which are inserted at every fifth pulse would be of the same sign, and a change of the sign of the recorded pulses would not occur until at the end of the word the positive word-end marker pulses appeared. Thus in this instance there would be as many as 50 negative pulses in succession, and if the Pulse Selector were to start its operation out of synchronism it would read all of these 50 pulses incorrectly as positives. This would throw the Indexer out of step, and the Word Count would become incorrect.

The situation can be considerably improved by adding a reset to the counter which every time that the magnetic wire is restarted so biases the counter that if the reproduced signal consists initially of an alternating sequence the counter will always read this as a series of negative recorded pulses and never as a series of positive pulses. (Then at the first change in sign of the recorded pulses the synchronizing feature will make the reading correct.) Under these conditions the maximum number of pulses which could be read incorrectly at the beginning would be reduced from 50 to 9; these 9 errors would occur in case a word ended with 4 positive pulses, followed of course by the 5 positive word-end pulses. Then if the wire were to be started at this point it could happen that these 9 positive pulses would be read as negatives.

In the event that the magnetic wire is restarted in the same direction that it was travelling before it stopped these 9 errors will have to be included in the approximately 27 errors which are permissible without causing the Indexer to lose count of the words on the wire. This would cut the number of pulses which can be lost during the stopping and starting of the magnetic wire down to about 18. If, however, the magnetic wire is restarted in the opposite direction, these 9 possible errors could cause an error in the word count even if no pulses were lost during acceleration.

It would be possible to add to the Pulse Selector and the Indexer extra circuits which would observe whether or not these synchronization errors occurred, and which would correct for them in case they did, but fortunately this is not necessary for the present work. In the present construction of an experimental but operating model of the computing machine ("Model O") it is



planned to restrict the operation of the input circuits to operation with groups of words, these groups of words being separated on the magnetic wire by a very considerable space, of the order of feet. Then the wire will always be started from one of these long spaces, reaching reading speed before the first pulse of the next group of words is reproduced. Under these conditions there is no problem either of synchronization of the Pulse Separator or of the loss of pulses during acceleration.

For the final machine ("Model 1"), it is suggested at this time that the plans consider the use of an "absolute" marker system for the wire, that is, a system which would contain location markers throughout the length of the wire permitting position identification without having to maintain a count from the beginning of the wire. The present system has no such absolute markers but operates on the principle of maintaining a high degree of reliability in the counting of the words on the wire. Two absolute systems are being considered at this time:

Scheme 1: This scheme permits ready conversion of the existing Indexer equipment. It consists of a.) the addition of 5 extra positive marker pulses at the end of each word, and b.) the insertion every so often (say every 256 or 1024 words) of a special word in which the above 5 extra pulses are negative rather than positive, and the data pulses of which specify the number of the next succeeding regular word.

Scheme 2: This scheme uses an entirely different system of marker pulses. Each word would be recorded on the wire with the group of

40 data pulses followed by a group of 4 negative pulses. Thus each word would require a total number of only 44 pulses on the wire.

Then every so often (say every 256 or 1024 words) would be inserted a word consisting of 44 positive pulses; immediately adjacent to which is a word in which the data pulses specify the number of that location.

In using either of these schemes there would be no need to store in the machine's memory the position at which the wire has been stopped; every time an order occurred to read a particular group of words on a particular wire, a sequence could be followed something like the following: Regardless of where the wire may have been stopped --- and indeed the control at this time has no information telling it just where the wire has been stopped --- it is started moving backwards. Then the control watches for one of the special words specifying location on the wire. As each of these location words comes along the control checks as to whether or not its location is greater or less than that of the first word which is to be read into the memory; if the location number is greater, nothing happens and the wire continues to move backwards at full speed, but if the location number is less, the direction of motion of the wire is reversed. In the reversing the reading equipment may or may not lose synchronism with the words on the wire, but in any case, it is brought back into synchronism by the first group of positive marker pulses. Then the control watches again for the special words indicating location, this time for the particular word having the location next lower than the word to be read; from that point on, it counts off words until the desired one is reached. As a check, after the desired number of words have been read, the control can watch



for the next group of positive markers and check that synchronism has been maintained until then; this would catch the error if for any reason there were to be the wrong number of pulses reproduced.

As has been mentioned, the first scheme would permit ready conversion of the existing Indexer equipment; it would also provide positive marker pulses for synchronization and checking at the end of every word; but in doing so it makes less efficient use of the wire than the second scheme. The first scheme requires that for every 40 data pulses there be recorded on the wire somewhat more than 60 pulses (each word would be 60 pulses long, but the rarer location words will add slightly to the average), while with the second scheme for every 40 data pulses only somewhat more than 44 pulses would be needed on the wire. This would have the same effect on the speed of reading data into the machine as though the wire speed were increased by the ratio  $60/44$  --- a not inconsiderable increase. The disadvantage of the second scheme is that synchronization can be achieved and checked less frequently than with the first, but the degree of reliability required for adequate operation of the input-output apparatus is so high that this less frequent inclusion of the positive markers may be entirely adequate. It should be emphasized that with the procedure outlined above the total number of reproduced pulses is checked for any segment of the wire that is being read into the machine. The only difference is that in the one scheme this check can be done word by word while in the other it can only be done for a considerable group of words. This could result in error if during this considerable group a number of spurious pulses were to occur which is just equal to the number of real pulses lost, but this is a higher order effect and a system so prone to errors as to make this probability appreciable would be much more erratic than evidence indicates to be feasible, and too

erratic for use in any of the schemes so far considered --- it would be necessary to include very elaborate checking schemes.

#### IV. ARITHMETIC ORGANS

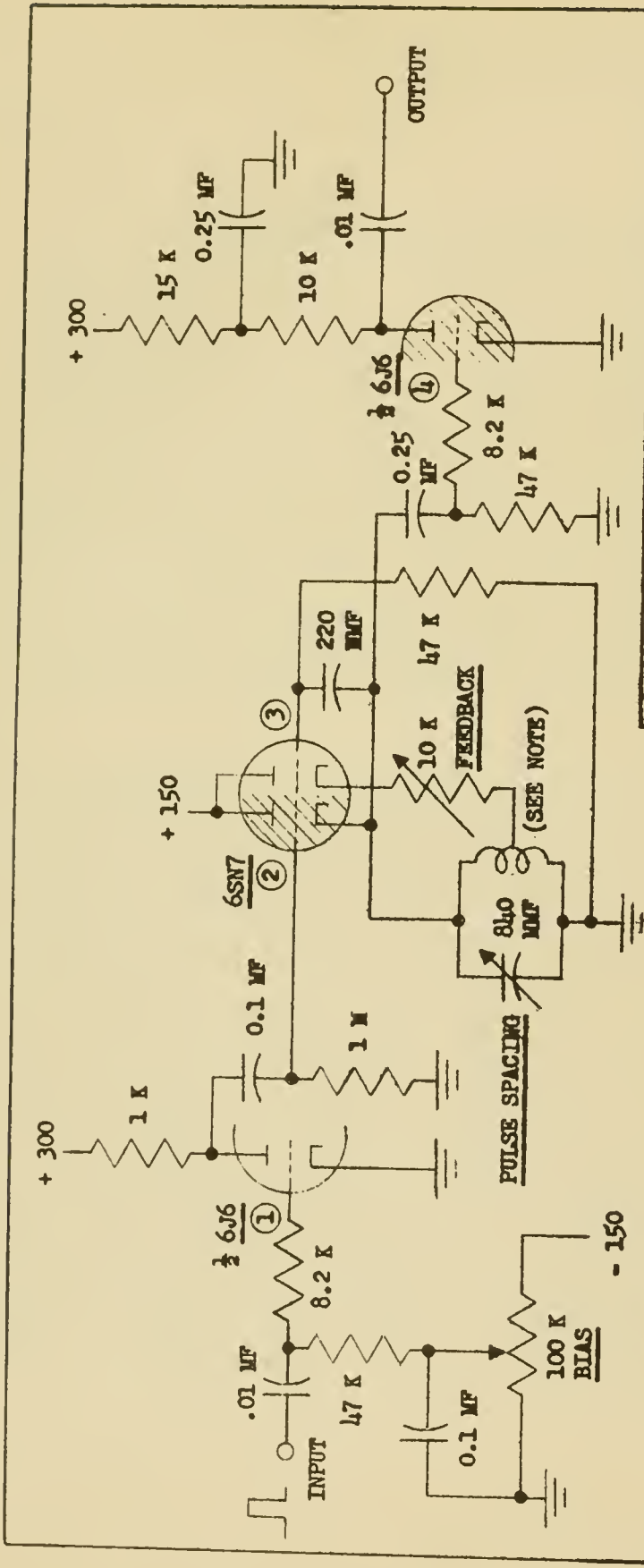
##### A. SHIFTING REGISTER

##### 1. Register No. 1. (Conditional Clear Type Shifting Register.)

The Conditional Clear Type Shifting Register was fully discussed in Progress Report No. 2, pg. 33; the life tests mentioned in connection with that discussion were made during the period covered by this present report.

The first problem in connection with this life test was to devise a source of pulses which would provide eleven equally spaced pulses separated by about one microsecond between adjacent pulses. A pulse source was available in the high-repetition-rate-rectangular-pulse generator, (drwg. C-2-1017, pg. 45a, Progress Report No. 2) and it remained to devise a trigger source for the pulse generator.

The unit devised was based on a range marker circuit well known as a component of radar equipment. (See Drawing C-2-1027, Pulse Group Generator, No. 2). Its operation is as follows: a positive pulse of variable width applied to the input is amplified and inverted by triode (1), and the resulting negative pulse is applied to the grid of triode (2). Triode (2), which is normally conducting, has in series with its cathode a parallel resonant tank circuit, which also forms the tank circuit for an oscillator tube, triode (3). While triode (2) is conducting, there is a large current flowing through the inductance of the tank circuit, and there is no oscillation. When triode (2) is cut off by the negative pulse on its grid, the tank circuit in its cathode return starts to ring, and the oscillation, supported by triode (3), continues until triode (2) is again



# NOTES

COIL - 190 TURNS,  
TAP AT 95° TURNS,  
ON 1 1/2" DIAMETER FORM.  
RESISTORS - 1/2-WATT, UNLESS  
OTHERWISE SPECIFIED.

## ELECTRONIC COMPUTER PROJECT

INSTITUTE FOR ADVANCED STUDY

PRINCETON, N. J.

PULSE GROUP GENERATOR NO. 2

C - 2 - 1027

DATE	DRAWN BY	CHECKED BY	INITIAL
12 - 11 - 47	H. HART	JWH	

returned to the conducting state, when the oscillations are quickly damped. The sinusoidal voltage developed at the cathode of triode (2) is coupled to triode (4) which operates as a clipping amplifier, and whose output consists of a string of pulses, sufficiently sharp to trigger the rectangular pulse generator without appreciable jitter. The number of pulses in the string is regulated by adjusting the duration of the input pulse, while the pulse separation may be varied from less than one microsecond to a maximum of about four microseconds by adjusting the variable condenser in the tank circuit.

Two outputs were taken from the rectangular pulse generator. The first, a positive pulse from the 50B5 toggle was coupled through an amplifier and pulse transformer to the clear bus of the toggle. The normal output of the pulser was coupled directly to the function bus of the register.

The pulser was set to deliver eleven pulses separated by approximately four microseconds, the groups being repeated at one millisecond intervals. A succession of digits was read into the register (01001011011), and the register was then pulsed for shifting. To the eye, of course, the register's glow indicator seemed to remain fixed in position, but observation by oscilloscope on one stage showed that the register was actually being shifted, for the sequence of the digits held in the register was shown by the scope.

Over a period of two and one-half weeks, the register was operated about eight hours a day. On some, but not all, of the days the register operated the whole day without showing any digits either lost or gained. When errors did appear, they were often the change of the digit in a single stage (and always the same stage) from 0 to 1.



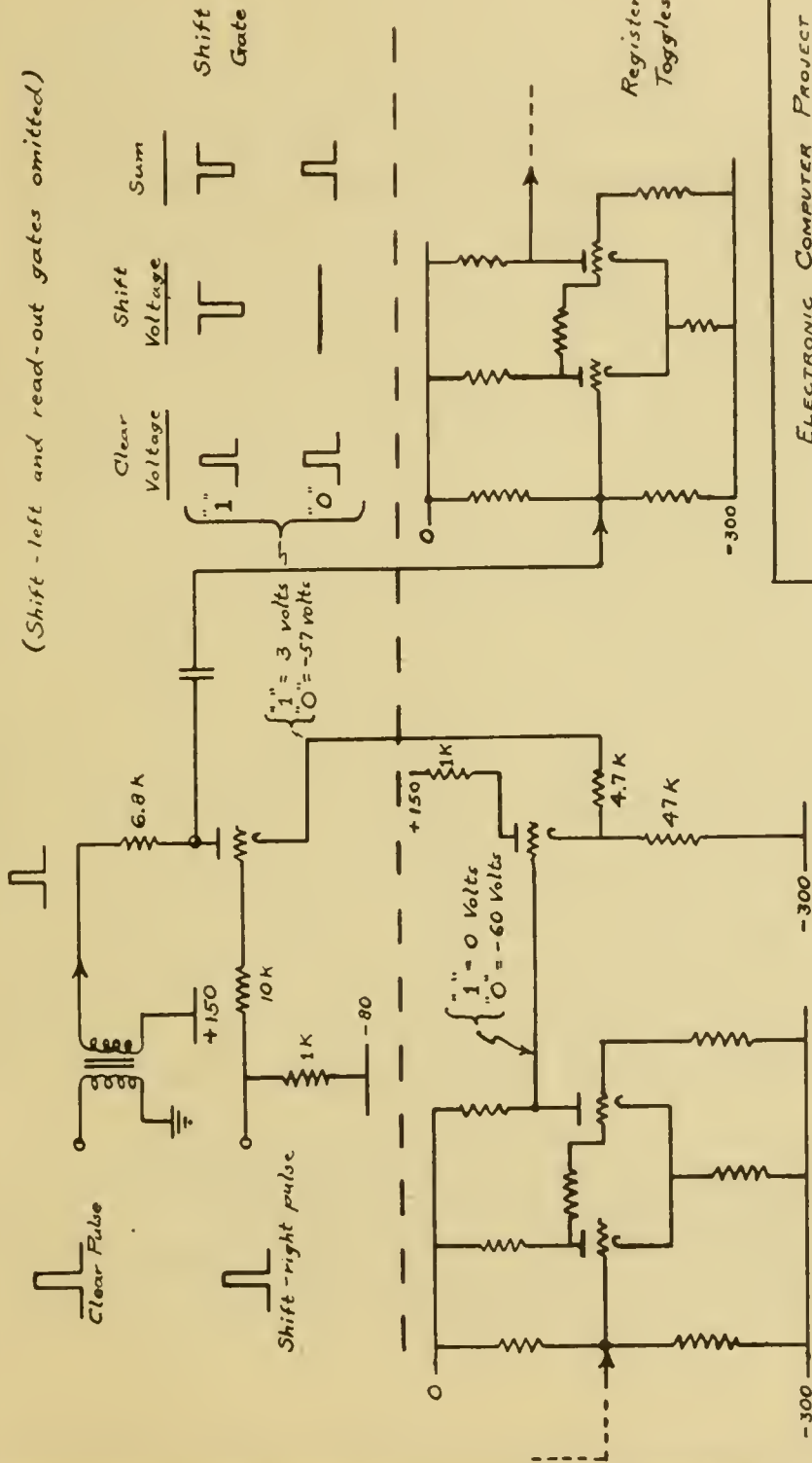
Prior to obtaining satisfactory operation of the register, it was found that about half of the 6.8 K resistors in the plate circuit of the read in gate tube, (left half of 2C51) had approximately doubled in value. The reason for the change in the values is not known, but the effect of the change was to make the clear voltage appearing at point A of some stages different from that appearing at others, since the resistor in question was directly in series between the clear bus and the point A, which is connected to the grid of the toggle. Upon replacing the faulty resistors with new ones of the proper values, satisfactory operation of the register was obtained. This unexplained occurrence has led to a present policy of measuring all resistors before insertion into circuits and again after wiring is complete.

The life test on the register and the laboratory work previous to it demonstrated the feasibility of single memory registers with transient digit storage for shifting, although a double memory type with positive, or steady stage, storage for shifting is now being used for its convenience in arithmetical manipulations.

Independent of this fundamental (transient storage) feature of Register No. 1 is the gating system used (see Drawing C-3-1028) in which a triode gate is controlled, that is, enabled or disabled, by driving its cathode from the free plate of a cathode-coupled toggle (through a cathode follower). To enact a shift, a positive pulse is applied to the grid of the appropriate gate while at the same time a positive clear pulse is applied in series with the gate plate resistor. If the gate happens to be disabled (controlling toggle at "0") the grid signal is ineffective and the positive clear pulse is transmitted through the plate resistor to the grid of the next toggle, setting it to "0".



(Shift-left and read-out gates omitted)



ELECTRONIC COMPUTER PROJECT  
Institute for Advanced Study  
Princeton, N.J.

GATING SYSTEM OF REGISTER No. 1  
C-3-1028

DATE: 12-23-47 DRAWN BY: J. P. Penagos CHECKED BY: JWS

If the gate is enabled (controlling toggle at "1") the grid signal produces a large negative pulse across the gate resistor which more than cancels the applied positive pulse, resulting in a net negative pulse on the following toggle grid, setting it to "1".

This gating scheme imposes several restrictions on the applied pulses. In particular the shift (grid) pulse must be large enough to drive the gate fully but not so large as to force it when disabled; also the clear pulse must be large enough to clear the following toggle when the gate is cut off but not so large as to reduce the net negative pulse below the threshold value when the gate is enabled. This balancing of the shift pulse against the clear pulse resulted in a practical range of 65-90 volts for the former and 45-60 volts for the latter for the present design. The clear pulse source is in series with the gate plates, so that it must supply a current per stage of either 0 (gate cut off) or 8 ma. (gate conducting). Since the number pattern can vary between all "0"s and all "1"s the clear pulse load variation is 0 to 88 ma. in the 11 stage register and would be 0 to 320 ma in the 40 stage unit. Maintaining the previously enumerated pulse amplitude limits against this variation required the development of very low-impedance, high-power pulsers even for the 11 stage unit. To minimize this trouble the subsequent register and adder designs (see IV B 1 a) were based on the principle that external pulse busses would not be required to supply plate or cathode currents, that is, only grids would be driven.

Another feature of this design which has been corrected in future designs is that pulses are transmitted from the gate tube to the toggles through condensers with no provision for d.c. restoration. Thus when shifting takes

place frequently a change will occur in the d.c. level of the pulse received by the toggle grid. This makes it difficult to strike a balance which will permit operation both at slow and at fast rates.

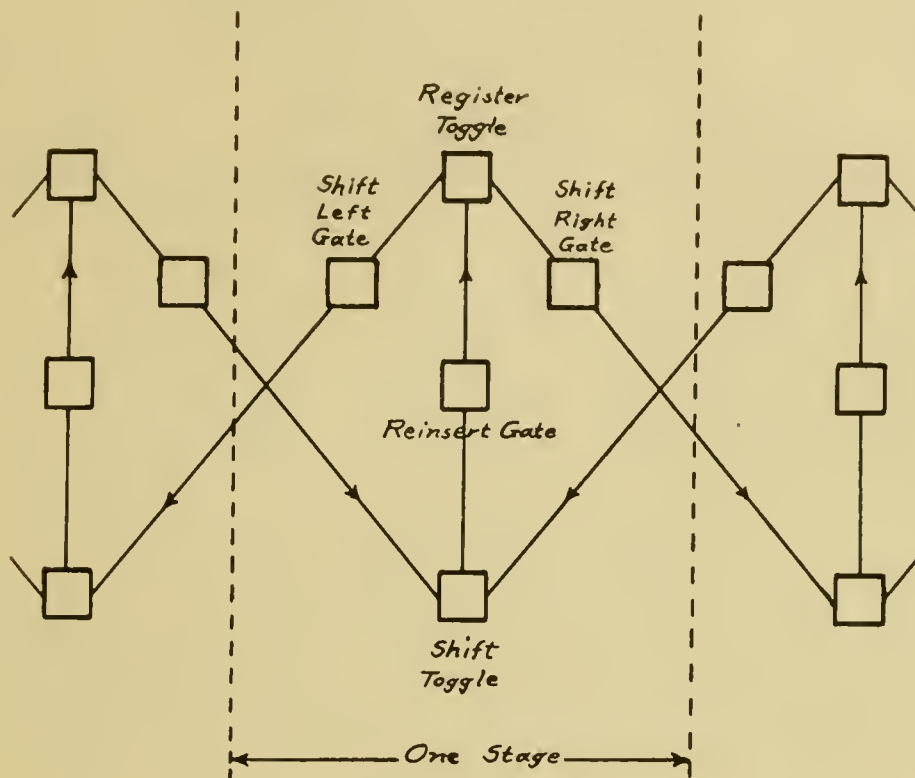
## 2. Register No. 3

a. Design This register was made of the "double register" type to take advantage of the ideas on the use of such registers described in the earlier progress reports. By "double register" is meant that there are two complete sets of toggles, called here the "register toggles" and the "shift toggles". Thus each stage of the register has one of each of these toggles associated with it, and a 40-stage register requires a totality of 80 toggles. In the process of shifting data is transmitted from one set of these toggles to the other, and only after its receipt in the second set is the first set cleared. Then the data is transferred back from the second to the first set, with the interconnections so made that it is now displaced one stage either to the right or to the left. This has the feature that while there is a minimum permissible duration for each of the shifting pulses there is no maximum limit, provided only that certain of the successive pulses do not overlap.

As also discussed in the previous reports, the number of tubes used in the physical realization of such a register may be reduced if the gates are simplified and able to transmit information of only one sign, being inactive if their inputs are of the opposite sign. Then the register receiving the information is in preparation cleared to read uniformly this "opposite" sign. Following the clearing the gates are pulsed, and they operate on the appropriate stages to bring the toggles to their correct values. Suppose, for example,

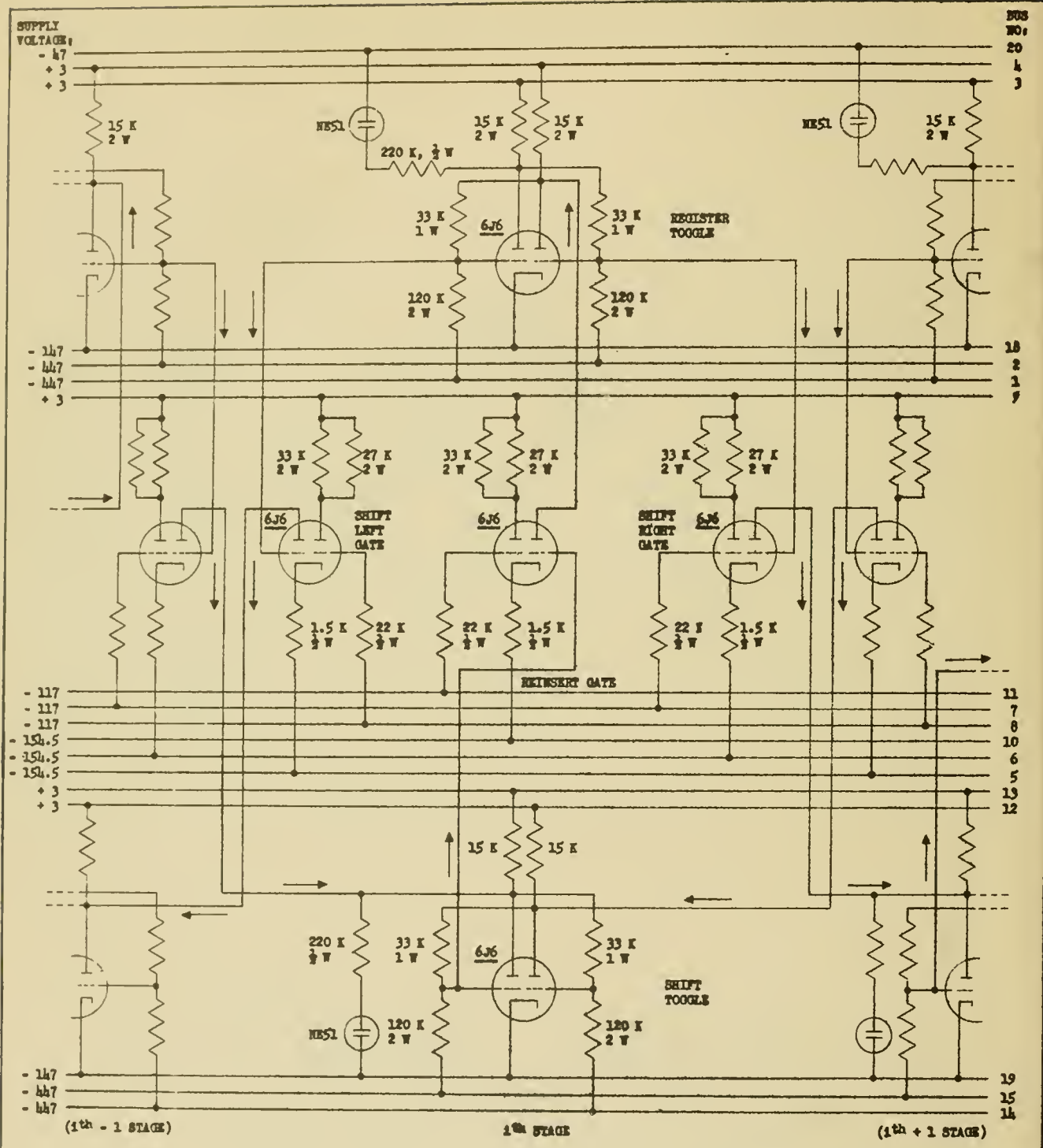
that the gates are arranged so that they will transmit "1" but not "0". Then to transmit information from the register toggle to the shift toggle it is first necessary to clear all of the shift toggles to "0". Following this the gates are pulsed and they turn the appropriate stages of the shift toggles back to "1". If the gates were pulsed without the inclusion of the clearing operation there would under certain circumstances be incorrect information left in the shift toggles after the operation, for any of them which should have been changed from "1" to "0" will have been unaffected. This type of register is known as a "clear-type double register" or a "4-pulse double register", since it requires four pulses to accomplish a complete shift (the four being "clear shift toggles", "transfer from register to shift toggles", "clear register toggles", and "transfer from shift to register toggles").

Shifting Register No. 3 is of this 4-pulse type. The interconnections between the various toggles are shown in Drawing C-3-1029. The connection of a gate to a toggle unavoidably introduces a loading on the toggle which is at best capacitive if not also resistive. In order to minimize this effect where two gates are connected to a single toggle they are connected symmetrically with one on each side of the toggle. This has the result that one of these gates will transmit only "1", while the other will transmit only "0". In this circuit the shift-left gate is of the former kind and the shift-right gate is of the latter, so the clearing operation on the shift toggles must be to all "0"s if a left shift is to follow, while it must be to all "1"s if a right shift is to be the following operation. The circuit of one stage of this register is shown in Drawing C-3-1021, with portions of the adjacent stages included to clarify the interconnections and loadings on the toggles.



ELECTRONIC COMPUTER PROJECT Institute for Advanced Study Princeton, N.J.		
SHIFTING REGISTER NO. 3 — BLOCK DIAGRAM C-3-1029		
DATE: 12-23-47	DRAWN BY: P. Panagos	CHECKED BY: JWH





ELECTRONIC COMPUTER PROJECT			
INSTITUTE FOR ADVANCED STUDY			
PRINCETON, N. J.			
SHIFTING REGISTER NO. 3: 1 <sup>st</sup> STAGE			
C - 3 - 1021			
DATE	DESIGNED BY	CHECKED BY	INITIAL
12 - 18 - 47	H. HART	JR	



The toggles in this register are of the symmetric type (the Eccles-Jordan type) which has for operation with the gates used here the advantage that the grid potential is limited in its positive traverse by the grid current which will flow whenever the grid potential at all exceeds that of the cathode. Thus the grid in its more positive condition comes to a rather well-defined potential regardless of considerable variations in resistor values or tube characteristics. This limiting of the grid voltage is used in the gate design to reduce the voltage range necessary for operation. In line with the design criteria described later in discussing the design of the adder, extensive calculations were made to determine what effect resistor and tube variations would have on the static operation of the circuit. It was assumed in the calculations that all resistors might change by 10%, with combinations of two or more resistors changing in the worst possible way. That is, if two resistors are connected in series to determine a potential at their junction it was assumed that one resistor might be 10% high in value at the same time the other was 10% low, or that it might be just vice versa. The tube characteristic was allowed to change by a factor of two; either twice as much for a given voltage, or else  $\frac{1}{2}$  as much.

Under these assumptions it was calculated that the plate potential of the tube would have a nominal high value of 103 volts above the cathode, with limits of 96 to 109 volts, while its nominal value with the toggle in the opposite state would be 29 volts, with limits of 15 to 52 volts. It might be noted that the limits on the lower state are much wider than those on the higher state because in the former the variations in the tube characteristic enter

as well as resistor variations, while in the latter only the resistor variations affect the result. The grid voltage was found to be always limited by the cathode voltage in the higher state, while its lower state had a nominal voltage of -42 volts with limits of -13 and -64 volts (again with respect to the cathode). The current drawn by the grid in its upper state had a nominal value 0.6 milliamperes with limits of 1.2 and 0.06 ma. The plate current necessary to be supplied by a gate tube to change the state of a toggle was nominally 2.5 ma with limits of 4.3 and 0.6 ma.

The gates used in this register are relatively unique for operating with both their grids and plates directly connected to the corresponding toggle elements ---- that is, with no need for any d.c. voltage translation either from the toggle into the gate or from the gate back into the toggle. This is accomplished with a double triode by returning the common cathode resistor to a voltage just 7.5 volts less than the cathode of the toggle. One of the triodes is used to disable the gate most of the time by pulling the cathode up to a voltage of at least 7.5 volts above the cathode. In this condition the second triode is always disabled because its grid is driven by one of the grids of a toggle and so is never appreciably positive of the cathode. When it is desired to activate the gate the grid of the first triode is pulsed negatively any amount below the cathode return of -7.5 volts. In this condition the second triode does or does not conduct depending on the grid potential supplied by the toggle. It will be remembered that this grid potential is definitely zero in one state of the toggle and definitely below -13 volts in the other toggle state. Thus the gate supplies current to its plate only at the

simultaneous command of both its activating pulse and its driving toggles. In the absence of grid current the gate will supply between 4.5 and 5.5 ma to the driven toggle to set it in the appropriate state if necessary.

It will be seen from the values quoted that the system appears highly reliable even under the worst combination of assumed component variations. Perhaps the weakest point in the design lies in the statement just preceding. "In the absence of grid current ---". If the gating pulse is made long, the plate of the gate tube will assume a very low value which may require that grid current flow in the gate tube to hold its cathode up to zero volts. This current would have to come from the grid connection of the driving toggle and it will be seen that if one is extremely pessimistic about component variations all adding up in the worst possible way, it would require only a small current drawn from the grid connection to change the state of the driving toggle. In this circumstance the information would be transmitted but the driving toggle would in the process be cleared and so no longer have the information. In shifting this would be of little consequence, but it happens that in addition it is necessary for the correct operation of the digit-recording gates to have the same information in both sets of toggles simultaneously. Some difficulty has been encountered from this effect in practice but it was eliminated by putting small resistors in the grid leads of the gate tubes. There are a number of other ways in which it can be alleviated, should it ever become necessary.

b. Tests. The tests of this register will be described in some detail, primarily to illustrate the effect of pulse shape on shifting speed, and

secondarily to illustrate the agreement between design value and those measured in the laboratory. The register was built in eight stages, using initially unselected tubes and resistors checked only for adherence to their nominal 5% tolerance. Note that a tolerance of twice this amount was used in the design; this is to allow for additional drift with age, and temperature.

Quiescent voltage measurements were made on all stages for both toggle states after replacement of three toggle tubes, for reasons described later, the toggles are nearly symmetrical, with fluctuations in potentials of the two sections of each toggle about equally distributed in each direction. The potentials of the non-conducting plates are uniformly +105 volts, while the conducting plates vary from +27 volts to +36 volts. The cutoff grids were found to fluctuate between -40 and -47 volts.

The enabling grids and cathodes of the gate tubes were consistently +11 to +11.5 volts in the non-gating condition. These were at least 11 volts above the transmitting grids, which ran no higher than +0.25 volt, and thus provides a cutoff bias for all normal 6J6 tubes.

From the time power was first applied to the register, all sixteen toggles were found to have two stable states. One NE-51 indicator neon lamp failed to function initially, and was replaced. All gate tubes shifted the proper signals, and all toggles cleared, when controls were applied manually through push-button switches described later. Dynamic operation with pulses on the order of a microsecond duration and 0.5 microsecond spacing indicated that three of the shift toggle stages were more difficult to clear than the rest. Measurement of the quiescent plate potentials in the "on" and "off" conditions indicated a greater unbalance on these than in the other thirteen



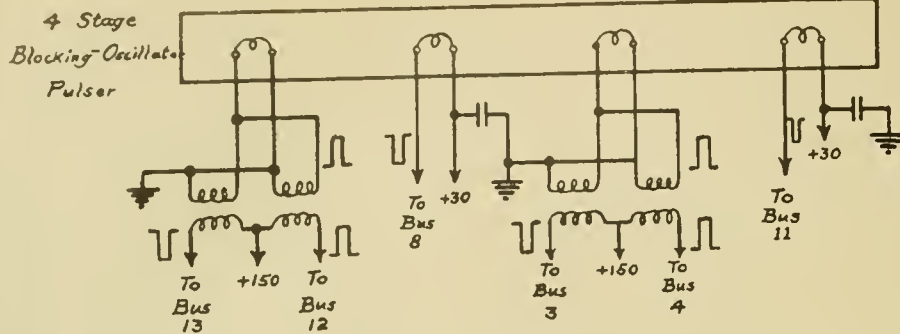
stages, by a matter of approximately five volts, i.e., the plate of a conducting triode was lower than the average of other similar conducting triodes by at least five volts. The three 6J6 tubes were replaced by new tubes, and failures to clear under conditions of close pulse spacing assumed a more random distribution. Because apparatus to measure the tube characteristics under different static conditions was not conveniently available, the cause of failure was not accurately determined. However, measurement of the  $g_m$  of the two sections of one 6J6 on the laboratory Precision Tube Checker showed a dissimilarity of approximately 15%. It is possible that the difference in characteristic under the conditions of use in this register may differ very considerably from this figure.

The toggles are statically asymmetrical mainly in the respect that an NE-51 indicator bulb is wired to one of the two 6J6 anodes. From a dynamic viewpoint, it may be seen from the schematic, Drawing C-3-1021, that there exists an unbalanced capacitive load on the register toggle because of a connection between the right-hand anode and the anode of the reinsert gate. Similarly, the shift toggle is unbalanced due to capacitive loading of the left-hand grid by the control grid of the reinsert gate.

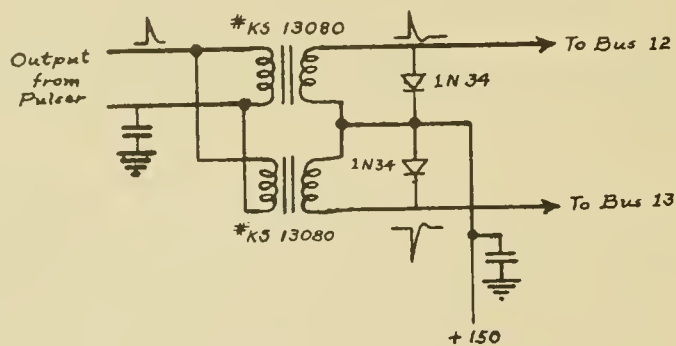
For dynamic or pulse operation, it is necessary that four pulses be supplied for a complete shift in either direction. The four-stage laboratory sliding pulser was used for initial testing. The pulses were applied as shown in Drawing C-3-1030(c).

The crystals used were type 1N34 specially selected to provide a back voltage of at least 80 volts for a back current of 500 microamperes. Since



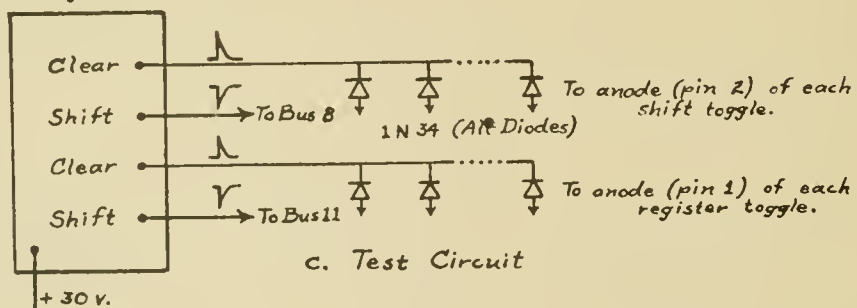


a. Clear Circuit



b. Balanced Pulser

Sliding Pulser



c. Test Circuit

ELECTRONIC COMPUTER PROJECT  
Institute for Advanced Study

AUXILIARY CIRCUITS FOR REGISTER No.3  
C-3-1030

DATE: 12-23-47

DRAWN BY: P. Panagos

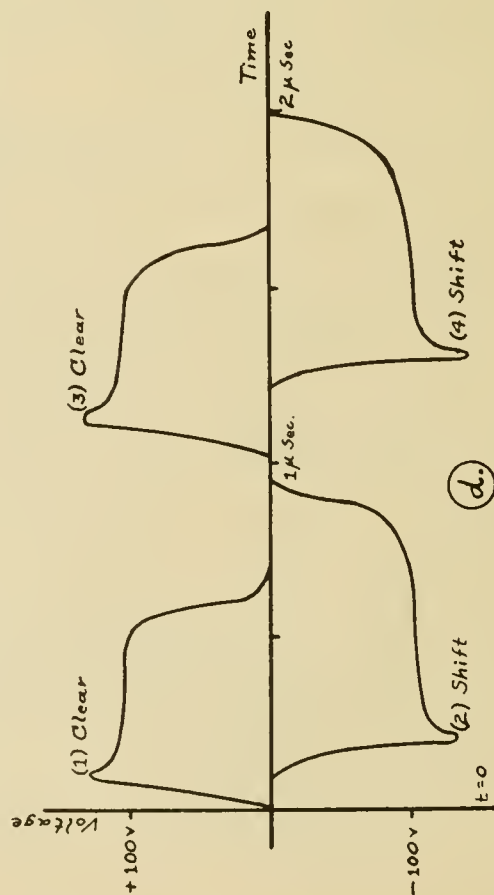
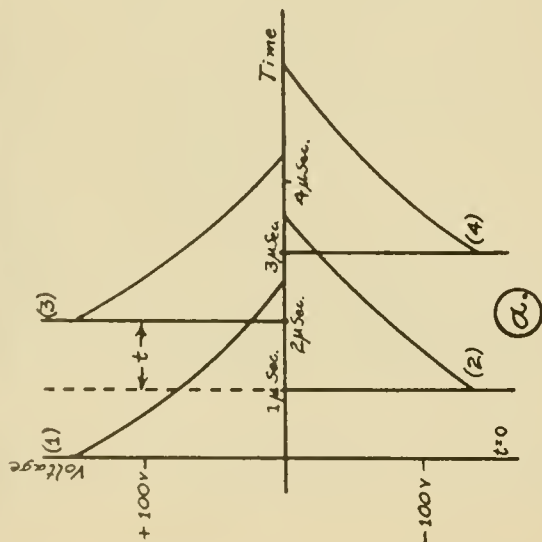
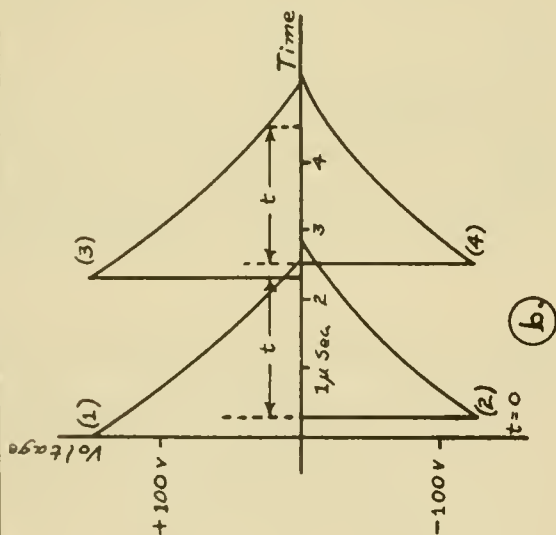
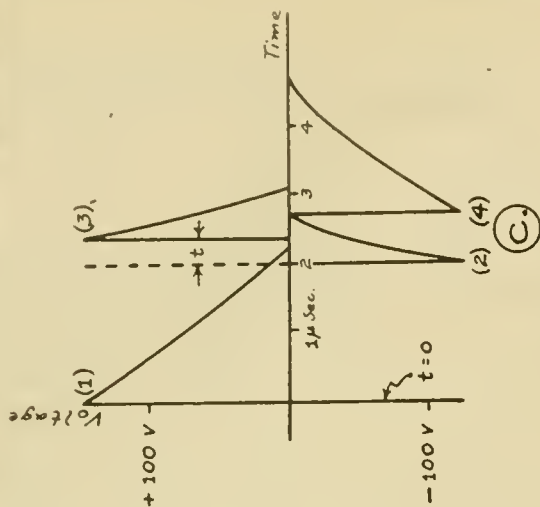
CHECKED BY: JWH

the quiescent voltage applied to bus 8 and bus 11 was to be +30 volts, it was expedient to have the pulser chassis returned to +30, and wire two outputs to the gate tubes. Except during the pulse, potentials on bus 8 and bus 11 were the same as on the chassis.

The crystals were wired to anodes of toggles which were +35 to +40 volts in the lower condition, and +108 to +112 volts in the higher condition. Thus no forward current was drawn except during the positive pulse output, and the maximum back voltage was 82 volts, at which time the crystal had a back impedance of at least 160,000 ohms. This provided minimum loading on the toggle circuit.

The pulses applied first were of sawtooth shape, with a very short rise-time of less than 0.05 microseconds, and an almost linear decay which had three different slopes. Pulse widths at 50% amplitude available by switching were 0.5, 0.3, and 1 microsecond.

Initially, stable operation was obtained only when each pulse was 1 microsecond long. Clearing was unstable for any pulse spacing when clearing pulses had a half-height amplitude of less than 60 volts. Shift pulses could be reduced to a half-height of 45 volts. Spacing for the train of four pulses is shown in Drawing C-3-1031(a). Stable shifting was available when the shift pulse was moved forward toward its preceding clear pulse almost to the point of coincident initiation. This was true of each shift operation. After the first clear-shift sequence, the next clear pulse, No. (3), failed to clear when the time "t" between the start of No. (2) and No. (3) was under 2 microseconds. When the pulse amplitude was reduced from the maximum of 150 volts, minimum "t" increased rapidly.



ELECTRONIC COMPUTER PROJECT  
Institute for Advanced Study  
Princeton, N. J.

PULSES FOR REGISTER No. 3  
C-3-1031

DATE: 12-23-47  
DRAWN BY: P. Panagos  
CHECKED BY: J. S. N.

The fastest stable sequence for a complete cycle of shift is graphed in Drawing C-3-1031(b). Pulse (2) is almost coincident with (1), but (3) may not be initiated for 2 microseconds after (2), and the first clear pulse of the next cycle, by extrapolation, could not begin within another 2 microseconds of the initiation of pulse (4). To include recovery time, therefore, a complete cycle required 4.5 microseconds.

It appeared that the chief limitation on shift speed was the slow decay rate of all the pulses, especially the shift pulses. Before pulse-shaping equipment was built, an alternate method of toggle clearing was investigated. This involved balanced clearing by application of equal pulses of opposite polarity on the two plate-return bus lines (+150 volts). Balanced clear pulses were produced with two identical transformers (see Drawing C-3-1030(b) ).

Thus the effective peak-to-peak clearing pulse was doubled, although applied through the 15000 ohm plate load resistors. This system had the further advantage over the former method that the crystal coupling diodes, with their capacitive and conductive loads, could be eliminated. That their conductive effect was important was shown by erratic results obtained when balanced clearing was first attempted. At this time no pulses were applied to the crystal coupling diodes, but their anodes were left connected in parallel, as before. The removal of all diodes eliminated the instability noted previously.

It might be mentioned that under the conditions in which these diodes were used it was possible because of finite back resistance for their common bus to assume a voltage within the range of voltages of the toggle elements to which the crystals were connected. No matter how high the back resistances

of these diodes might be, if the toggles were to remain quiescent for a long enough time with the right number pattern in them, this condition could occur. If it occurred some of the toggles being cleared would find themselves loaded with the full capacity of the common diode bus, and it is not surprising that clearing should be sluggish or erratic. A similar situation arises in the circuit used for the recording gates of Accumulator No. 7. There the difficulty was anticipated and prevented from occurring, as described in section IV B 2 b.

Balanced clearing permitted a decrease in width of pulses (2) and (3) to 0.3 microseconds, and a decrease in the time "t" noted previously to 0.2 microseconds. However, pulses (1) and (4) remained at a width of 1 microsecond for stable operation, and pulse (2) could not be initiated until pulse (1) had completely decayed. It was reasoned that the shift toggles did not become stable and receptive to a shifted digit until the clear pulse was removed. When pulse (2) had the same decay slope as pulse (1), shifting occurred when the two overlapped, providing pulse (2) ended 0.2 microseconds or 0.3 microseconds later. A new shift cycle was now possible; indicated in Drawing C-3-1031(c).

The considerable reduction in the time "t" as a result of the rapid decay of shift pulse (2) led to the belief that if rectangular pulses were available, shifting speeds could be considerably improved. For this, a pulse-forming blocking oscillator, delivering fairly rectangular pulses of width 0.3, 0.5, and 0.7 microseconds was built for each of the four pulses.

Results obtained from the use of rectangular pulses confirmed the previous belief. Balanced clearing was employed, as shown in Drawing C-3-1030(a). It was again found that the shift pulse could begin before the clear pulse had ended. For most stable operation, shift-pulse widths were kept at 0.7



microseconds, while clear pulses functioned at 0.5 microseconds width.

Refer to Drawing C-3-1031(d) for the sequence.

At this time the major speed limitation seemed to be the wide shift pulse. In an attempt to improve shifting, all cathodes of similar gate tubes were wired in parallel. By so doing, it was felt that the shift speed of the slowest gate tubes would be aided, since the cathode current of the fastest gates would be switched-off to the transmitting grids remaining in the most positive condition. This improved the shift cycle from 2.5 microseconds to 2 microseconds. The 2 microsecond shift sequence was tested for stability for periods up to two hours, and found satisfactory. For short periods, the clear pulses could be compressed to a width of 0.3 microseconds and the sequence to 1.5 microseconds, but they were not completely stable. Stability of shift became dependent on the digit pattern initially impressed; the most unstable patterns used were seven 1 digits and a 0 digit, or seven 0 digits and a 1 digit. One dissimilar digit had to be included because failure could result either in the production of all 0 digits or all 1 digits, depending on whether failure to clear occurred in the register toggles or the shift toggles.

An examination of the wave-form of the shift pulse on the enabling grid of the gates showed that this pulse had a rise time of 0.2 instead of 0.1 microseconds. This was probably caused by a combination of the 22,000 ohm series grid resistor (limiting quiescent grid current) and the parasitic grid capacitance to ground. At a later date this resistor will be bypassed with a capacitor in an attempt to improve shift response.

Conclusions Within the limitations imposed by the use of a two-register type of shifting register, it is felt that this register operates satisfactorily. It can be stable at high shifting speeds, but fairly high stability of pulse spacing and good control of pulse amplitude and waveform will be required.

A train of four pulses is necessary for a shift in either direction, while a sequence of five will be needed to accomplish a stage of multiplication and nine for addition in conjunction with the adder to be used. The register is reasonably undisturbed by variation of normal components, and it is believed to be quite stable with respect to small supply voltage drifts. Of unique interest is the so-called "D C" method of shifting, wherein no change in the D C voltage level from transmitter to receiver occurs. Condenser coupling is nowhere employed. Stability is emphasized throughout, at some expense in convenience of operating controls. Where the total time in continuous duty of a shift plus recovery need not be less than 3 microseconds, it is believed that this unit will be quite acceptable.

### 3. Single vs. Double Registers

Considerable qualitative discussion has been presented in the previous progress reports concerning various kinds of shifting registers. Recently there has been developed a semi-quantitative analysis of the problem which is of some interest. When one is considering the operation of a shifting register at rates which are slow compared to its maximum capabilities it seems obvious that a system in which there is time-dependent storage of the information during the shifting process (a "single register") will be less reliable than a system in which there is at all times a statically-stable element containing the information. (This latter system is called here a "double

register" because it involves in essence the inclusion of two toggles for each stage of the register.) A single register requires that the gating signal be longer than a certain minimum time necessary for operation, and at the same time shorter than a certain maximum time determined by the characteristics of the time-dependent transitory storage. On the other hand the gating signals of a double register will have about the same minimum time, but no maximum time whatever, subject only to the provision that certain successive gating signals should not overlap each other. The information is always locked in one or the other of the toggles and cannot be lost because of time-constant effects.

When, however, the registers are operated at speeds comparable with their maximum, it may be argued that the situation is by no means clear. Then every operation will be allowed a minimum of time consistent with the desired reliability as affected by uncontrollable variations in individual elements, and in such a case it may be possible so to design the minimum and maximum times for a single register that the same reliability is held as for a double register constructed of the same type of toggles and gates, but still have the single register operate more quickly. If this were so, and it were desired, it would obviously be also possible to perform the converse and have the single register shift as rapidly as the double and yet with greater reliability - - - the uncontrollable variations in individual elements would have a smaller probability of causing failure. To understand this argument consider first a single toggle. Whatever means of setting this toggle is used there will be a certain minimum duration of pulse necessary. Take this, for an example, as 0.75 microseconds. This value might be true for a single toggle with



pulses of one particular amplitude and shape, but it will vary slightly from toggle to toggle even if the pulses are kept constant. It would be most unsafe to design equipment in which this kind of toggle received pulses of just that duration and amplitude. The designer will have to provide for possible variations from toggle to toggle, and the width of the variation which he will provide for will depend on the degree of reliability to be achieved. There may be no quantitative data on the statistical variation among a large number of toggles with different supplies and at different times, but the permitted variation will increase with an increase in the desired reliability. Suppose that it is decided that a variation of 2:1 is to be expected under the conditions of application, then if the value of 0.75 microseconds is taken as an average in the design the duration of this pulse necessary to operate the toggle would be considered to vary between 0.5 and 1.0 microseconds. Then to operate with the required reliability the design should see that toggles of this type always receive pulses of duration at least 1.0 microseconds. However, variations will occur also in the pulsers, and if the same variation were to be allowed, the pulser should have a nominal value of 1.5 microseconds and be expected to remain within 1.0 and 2.0 microseconds with the given reliability. The important thing is that there is such an upper value below which the pulser may be expected to operate with a reliability consistent with the rest of the design. If now the transient digit storage consists of a delay with this same value as its lower limit it only remains to see that the next gating pulse doesn't start before the upper limit of the delay element, and shifting will be achieved with the specified reliability. If the same assumption of 2:1 variation is continued the delay element would have expected limits of 2.0 and 4.0 microseconds, and the next

gating pulse should arrive at a nominal 6.0 microseconds, the expected limits being 4.0 and 8.0 microseconds. The average shifting cycle would then be the 6.0 microseconds, since the next cycle may be timed from the actual time of occurrence of this pulse.

Thus the basic idea of the analysis is that although there is a maximum limit to the pulse duration for a single register, under certain circumstances such a register may be so designed that this maximum limit is achieved with the same reliability as is achieved the minimum pulse duration limit inherent in both the single and the double registers. This is true whether the "reliability" is measureable numerically or whether it is obtained by limits set as a result of engineering judgment. Once the reliabilities are made equal it can be determined which scheme operates more quickly.

These considerations have been carried out in general form for single registers, for "2-pulse double registers" (where the gates are arranged to transmit both "0" and "1" so that it requires two gating pulses to complete a shift cycle), and for "4-pulse double registers" (where the gates transmit for only one state of their driving toggles, and it is accordingly necessary to have two clear pulses as well as the two gating pulses to complete a shift cycle). Assumptions made are:

- a. The same ratio,  $R$ , is to be allowed between the maximum and the minimum times for all elements of the circuit. If  $R$  were considered to be different for different elements the analysis would be similar but would be somewhat more complicated.
- b. Pulses are assumed not to overlap each other. They may, however, be used to signal the start of the next pulse whenever that is



appropriate to the operation of the circuit. Thus it is assumed in the double registers that the cessation of one pulse is used as a signal for the start of the next. With this the contribution of such a pulse to the total cycling time becomes its average value rather than its maximum limit.

- c. Reliability as referred to here applies only to failures caused by variations which may occur in the time of operation of the various elements of a circuit. It does not consider the possibility of a total failure of an element such as would be caused by failure of the heater of a vacuum tube. Such possibilities would be expected to increase as the total number of elements in the circuit increases, so circuits indicated as equivalent by this analysis should in reality favor the one with the fewer elements.

The variables entering into the analysis are:

- T , the pulse duration necessary to set a toggle in the desired state,
- G , the actual duration of the gate pulse applied to set the toggle into its new state (G does not appear explicitly in the results.),
- N , the time, measured from the start of T, when the gate on the output of the toggle receives the information of the new state and is prepared to gate accordingly,
- R , the ratio which is to be allowed between the maximum and minimum times for all elements of the circuit.
- C , the time for the completion of one shift cycle and up to the start of the next.

T, G, N, and C can all be considered either the minimum, the maximum, or the

average allowed time provided it is the same for all of them, but C is most significant if it is expressed as the average time for one cycle, in which case all the others should also be average times.

The solutions have different forms, depending on the value of the ratio  $N/T$ . They are:

Register Type	If	Then	
Single	$\frac{N}{T} \leq R^2$	$\frac{C}{T} = R^3$	
	$\frac{N}{T} > R^2$	$\frac{C}{T} = R \frac{N}{T}$	
2-Pulse Double	$\frac{N}{T} \leq 1$	$\frac{C}{T} = 2 R$	
	$\frac{N}{T} > 1$	$\frac{C}{T} = 2 R \left( \frac{N}{T} \right)$	
4-Pulse Double	$\frac{N}{T} \leq 2$	$\frac{C}{T} = 4 R$	
	$\frac{N}{T} > 2$	$\frac{C}{T} = 2 R \left( \frac{N}{T} \right)$	

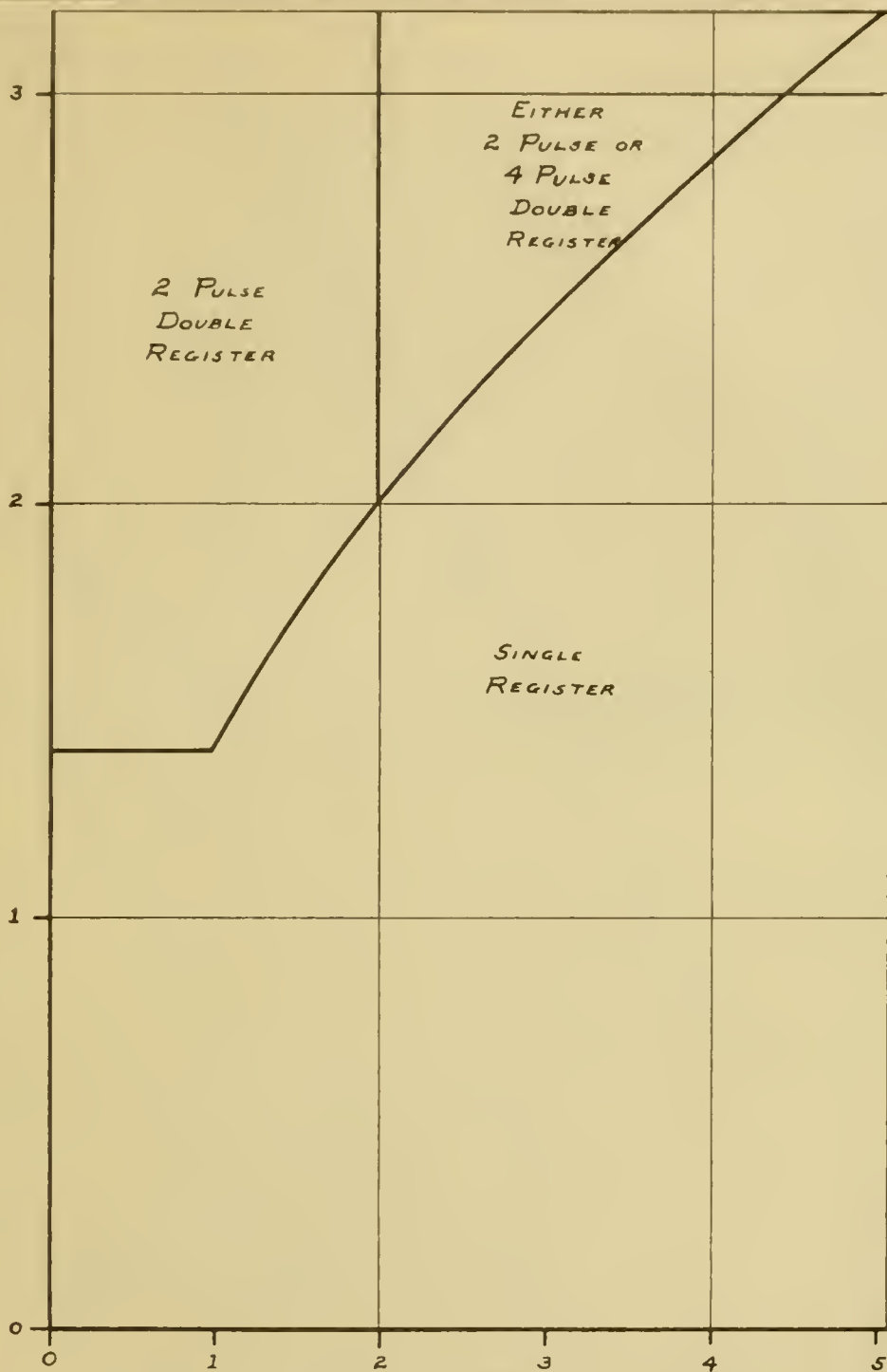
A set of these solutions for the particular case of  $R = 2$  is plotted in Drawing C-3-1033. It may be seen that for this case if  $N/T$  is less than 2 then the 2-pulse double register will shift more quickly with the same reliability as the other registers, while if  $N/T$  is greater than 2 the single

register will be the better. It is interesting to note that for this case if  $N/T$  is 2 then all three registers would be equally reliable according to this analysis. This value of 2 for  $N/T$  is of the same order of magnitude as has been observed for many of the toggle and gate combinations tested in the laboratory.

The above general results have been solved to determine which kind of register will give optimum results for a given combination of  $R$  and of  $N/T$ . The results are shown in Drawing C-3-1034. With, for example, an  $R$  of 2 and  $N/T$  of 1, the 2-pulse double register will give optimum performance. That is, it will give greater speed than the other register types with equal reliability, or, if so designed, it will give equal speed with greater reliability.

Some consideration has been given to the effect of permitting successive pulses to overlap whenever it would not produce a false signal on a gate. Thus the clear and shift pulses might be partially overlapped in the 4-pulse double register. The effect of this on the curves plotted would be to extend the diagonal portions of the curves, lowering the horizontal portions accordingly and moving the vertical line in C-3-1034 to the left. This applies to the curves in both drawings, with the exception of the curve for the single register in C-3-1033, which would remain unchanged.

$R = \text{Ratio of Max. to Min. Time for All Elements}$



$\frac{N}{T} = \text{Ratio of Gate Activation to Toggle Pulse Time}$

ELECTRONIC COMPUTER PROJECT  
Institute for Advanced Study  
Princeton, N. J.

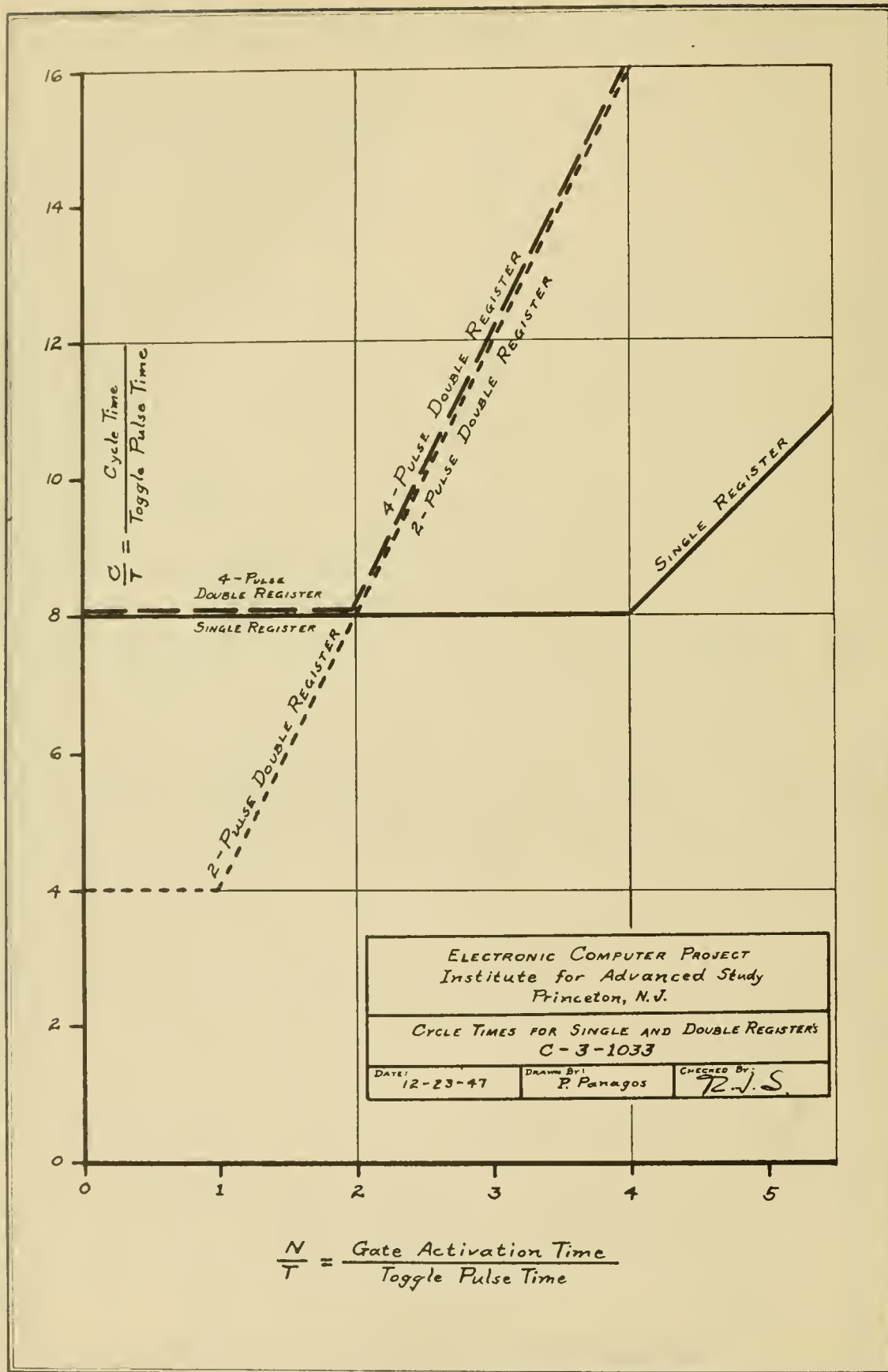
OPTIMUM REGISTER TYPES

C-3-1034

DATE 12-23-47

DRAWN BY P. Panagos

CHECKED BY J. J.





## B. ACCUMULATORS

As discussed in Progress Reports Nos. 1 and 2 (1 January 1947 and 1 July 1947) the accumulator may conveniently be considered in two parts: (1) the accumulator register and (2) the adding circuits. The accumulator register provides statically stable storage for 40 binary digits, is able to shift its stored number either left or right, and is able to receive or read out its 40 digits in parallel. It furnishes one of the two number inputs to the adding circuits, that is the resident (R) number. The adding circuits form the sum of the resident number and a number presented from outside the accumulator, the incident (I) number, and impress this sum on the record gates for gating back into the accumulator register. In addition it is convenient to consider as part of the adder a set of complementing, or Add-Subtract, gates which operate on the incident number and present either the number or its complement to the adding circuits.

The accumulator register may be any one of several types of shifting registers whose general characteristics have been discussed previously. Some further discussion of the adder will be desirable however.

The two numbers applied to the adder may give rise to carries in any of the 40 stages so that a particular digit place, or stage, must form the sum of not only the R and I digits but also a carry digit (C) from the preceding stage. The output will consist of the new resident digit  $R'$  and a carry digit to the following stage. Certain fundamental considerations concerning C and  $R'$  should be stated here. (a) Since the new resident number  $R'$  is not complete until all carries have been completed it is necessary either to detect the

completion of carries or always to allow enough time for a carry to propagate through all 40 stages. If the latter course is used it is particularly important to maximize carry speeds. (b) Also, since the sum is to be deposited in the accumulator register, hence obliterating one of the constituents of the sum, it is necessary either to provide delay between the R input and the record gates or else provide an intermediate memory in the record operation. Both systems are illustrated in circuits to follow.

#### 1. Accumulator No. 2 (Double Kirchhoff Summation Type)

a. Design The previous progress report described an accumulator particularly designed to maximize carry speed. (See Fig. 49 of Report No. 2). This is referred to as a "Kirchhoff summation" accumulator because the process of addition is carried out by superimposing standardized voltages and currents on a linear resistance network, thus generating a voltage whose amplitude represents the sum being formed. In Accumulator No. 2 this summation is performed once to determine the new carry digit and then again to determine the new resident digit  $R'$ . The digits of the numbers to be added are introduced as constant currents of either 0 or 8.0 ma corresponding to "0" or "1". These currents are drawn from the bottom end of a 3.0 K summing resistor, the top end of which is supplied with a constant voltage of either 0 or -24 volts corresponding to "0" or a "1" carried over from the preceding stage. The two digits and the carry produce four possible voltage levels at the bottom end of the summing register, each 24 volts lower than the next (i.e. 0, -24, -48, -72).

The carry is introduced as a voltage step rather than a third current step as a result of carry-speed considerations. Each binary stage of this

accumulator was built as a separate plug-in unit and it was desired to route the stage-to-stage carries through one set of the plug contacts. The 8 ma standard current would charge the resulting capacity only slowly; accordingly the standard voltage step was adopted and supplied through the substantial current amplification provided by a TS-229 cathode follower.

The first Kirchhoff summation is seen to yield a 4-level voltage proportional to the number of incoming "1"s but independent of their various permutations:

No. of incoming "1"s		Summing Point Voltage	Carry Output	New Resident Digit (R')
Decimal	Binary			
0	00	0	0	0
1	01	-24	0	1
2	10	-48	1	0
3	11	-72	1	1

The summing point voltage is applied to a cathode follower whose load consists of a resistor and a constant current pentode (6AQ5) in series, the function of this combination being to reduce the d.c. level of the steps by a constant 110 volts. Thus the translated voltages are ideally -110, -134, -158, -182 although in practice the intervals are somewhat decreased.

The carry-output digit is determined from the translated summing-point voltage by a double-triode cathode-coupled gate set to open between the 1 and

the 2 incoming digit level. The negative output of this gate gives the carry directly, and is applied to the grid of the cathode follower previously described. Note that the voltage translation permits the gate plate to operate from 0 (cut off) to -24 (conducting 8 ma through 3 K) which is the proper level for the carry to the next stage.

The new resident digit ( $R'$ ) is determined from the positive output of the carry gate and the original summing-point voltage by a second Kirchhoff summation according to the formula

$$R' = N - 2C$$

$N$  = number of incoming "1"s

$C$  = carry digit

so that the positive output of the carry gate is required to be either -48 ( $C = 0$ ) or 0 ( $C = 1$ ). The result of this second summation is amplified and inverted and applied to the recording gate. The parasitic capacities in the system are sufficient to provide the necessary delay.

The accumulator register consists of a cathode-coupled toggle with conditional-clear-type shifting gates, where a large negative digit pulse (on for a "1", off for a "0") is balanced against a smaller positive clear pulse and the sum applied to the left grid of the following toggle.

b. Test Eleven stages of Accumulator No. 2 were built, each stage being a separate strip with d.c. and pulse voltages supplied through Jones plugs. An eleven-position rack was constructed to integrate these units (See Fig. 49 Progress Report No. 2). Carry and shift connections were made directly between stages.

A deliberate attempt was made in the design to minimize the number of external supply voltages; these were restricted, in fact, to +150 and -300 (and 0).



Intermediate voltages were supplied by individual voltage dividers on each stage. In practice it was found that resistor tolerances compounded severely in the case of the d.c. translation circuits, the gating-level voltages, and the left-hand toggle-grid supply voltage, making it necessary to adjust each divider separately to keep variations within limits. After the initial adjustment, occasional further adjustment was needed to correct for small resistor drifts over a period of a day or so.

Pulse tests were made following the d.c. adjustments; here again individual corrections of (gate plate) resistors being necessary to permit operation of all 11 stages at the same pulse amplitudes. The following speed and pulse-voltage limits of operation were obtained:

Carry time .05 microseconds per stage

Clear pulse range 56 - 71 volts

Record pulse range 28 - 47 volts

Shift-rt.pulse range 38 - 65 volts

Shift-left pulse range 43 - 64 volts

The characteristics of the record and the shift gates were found to be sufficiently similar that shifting could be done reliably as soon as the record function was adjusted. Various add, shift, and multiplication sequences were tried using manual control of the pulsers, and correct answers obtained.

c. Conclusions Whenever proper d.c. and pulse voltages were achieved, this design functioned satisfactorily. In particular the carry time was very fast; extrapolated for 40 stages it would be between 2.0 and 2.5 microseconds. It was too critical, however, with respect to normal resistor drifts and pulse



voltages, the former being very serious with respect to the d.c. translating circuit and the second Kirchhoff summation and the latter being particularly difficult to maintain constant because of wide variations in lead with the number pattern dealt with.

## 2. Accumulator No. 7

a. Adder In the reports which have preceded this there have been discussions of the logical aspects of providing for the propagation of a carry through several stages, and it has been pointed out that if means are included for determining the completion of a carry propagation it is possible to terminate the addition then and so to use in the addition only that time necessary for each particular case. With this the average time required for addition becomes that for the propagation of an average carry sequence rather than that for the maximum carry sequence. It must be remembered, however, that at the best the inclusion of means for sensing the termination of the carry process adds to the complication of the electrical circuit ---- in fact, many such schemes also actually slow up the carry propagation, so the time gained would be cut down by this slowing up. The construction of Accumulator No. 2, then, served to prove that by careful attention to circuit details the propagation of the carry from one stage to the next could be made sufficiently rapid that a balanced design could be achieved without the necessity of sensing the carry termination. In that design a carry could travel all of 40 stages in not more than 2.5 microseconds; thus only a time of the order of a microsecond or two could be saved by shortening this time, and such a saving would be of little value in view of the estimated times for the other operations of the machine.

On the other hand, that circuit was designed primarily to determine just the point of the carry speed, with much less attention to the question of reliability. This by no means implies that carry speeds that great are inconsistent with good reliability, but merely that in the interest of determining the point expeditiously. Accumulator No. 2 was designed with the reliability problem definitely left to a secondary role. Having settled that sufficient speed could be obtained in such a static adder, a new design was started in which the strong emphasis was on reliability; while carry speed, although still important, was subordinated. The aim was to achieve a design in which the overall reliability of the circuit would be greatly improved, although the carry might turn out to be a bit slower. The experience with the previous model was embodied in a comprehensive set of design criteria:

1. The average power dissipation in the plate or grids of a tube should not exceed 50% of the rated ("absolute maximum") dissipation.
2. The average cathode current should not exceed 50% of the rating, and the peak cathode current should not exceed the rating.
- 2a. The maximum current drawn from a crystal diode should not exceed  $\frac{1}{2}$  the rating.
3. The maximum voltage between elements should not exceed  $\frac{2}{3}$  of the rating.
- 3a. The maximum back voltage applied to crystal diodes should not exceed  $\frac{1}{2}$  of the rating.
4. The so-called 50% emission criterion:

The circuit should continue to operate satisfactorily even if the vacuum tubes deteriorate to the point where for a given set of voltages applied to the electrodes the currents produced are as low as 50% of the values specified in the published tube characteristics.

- 4a. When a tube is operated with the grid positive and drawing a specified current, the circuit should permit variations of the plate (and screen) volt-ampere characteristic lying within factors of  $\frac{1}{2}$  and 2 times the average characteristic observed for new tubes.
- 4b. The circuit should operate satisfactorily if the back resistance of crystal diodes were to fall to  $\frac{1}{2}$  of the minimum back resistance permitted for the crystals as installed in the circuit.
- 4c. The forward resistance of crystal diodes should be permitted to increase to twice the value as installed.
- 5. The circuit should work satisfactorily even if all resistors differ from their design value by as much as 10% in either direction.
- 6. Use the minimum feasible number of tube elements.
- 7. Have the individual parts of a circuit as nearly independent of each other as possible.
- 8. Use no balancing of one pulse against another either to cancel the two out or to override one by the other.
- 9. Have no amplitude discrimination on pulses. Consequently, have no spurious pulses which are expected to be rejected because of their small amplitude.
- 10. Use no discrimination between a desired and an undesired signal through use of time constant characteristics.
- 11. Do not pulse a load consisting of a number of elements whose reaction depends on the information stored in the machine; that is, do not pulse a number of plates or cathodes in parallel if the current drawn by these elements depends on the particular number stored in the machine.
- 12. Whenever pulses are transmitted through condensers, d.c. restoration must be provided so that the transmitted pulse should be essentially independent of duty cycle.

13. Voltages brought into a circuit from external power supplies may be considered to be regulated to within 1 volt if necessary.

It should be made clear that these criteria have not been used in any sense of absolute rigidity. While it is in the large number of cases possible to satisfy every item, there does occasionally arise a condition where the strict application would result in a structure so cumbersome that the mere multiplication of the number of elements in the circuit would result in an estimated probability of failure that would surpass that resulting from using a simpler circuit which might deviate from these criteria. Our use of these statements, then, is that any violation of them is a priori undesirable, but not strictly prohibited; it can be utilized but requires individual justification for the decision.

Let us consider some of these criteria. The limitations they impose on power dissipation in the tube elements are almost obvious; the need for long life in computer operation leads toward operation with as conservative temperatures as possible. The 50% emission criterion is intended to make allowance both for manufacturing variations in the tubes and for the gradual weakening which results as the tube ages. It would be very difficult indeed to set any design limit which would directly relate to the condition of the emissive cathode ---- indeed it is most difficult even to make a rational measurement of the state of the cathode emission ---- consequently resort is had to a purely phenomenological approach.

In (4a), a special condition is imposed for tubes operating with a constant current drawn from the control grid by the external circuit. In



this condition, the circuit is such that aging of an individual tube is to some extent counteracted. Consider a tube having fixed potentials applied to all elements except the control grid, while the control grid is attached to a positive voltage through a relatively high resistor. In this condition the grid will draw current, and since it takes only a few volts to draw relatively large currents to the grid, the grid will be only slightly positive. Now if the tube ages to the point where the 50% emission condition is reached, constant voltages on all the elements will produce only half the amount of current as formerly, however, this will cause the grid voltage to increase because there is less drop through the grid resistor. In fact, if the voltage applied to the grid resistor is large compared to the former positive voltage of the grid, the grid will increase in voltage until very nearly the same current is being drawn by it as formerly. To a first approximation this change in the grid voltage will very nearly produce the same proportional change in the current to the plate, so the plate current will be kept somewhere near what it was when the tube was new. Thus there has been only a relatively small change in the current drawn through the tube. However, in this circuit, while variations in the condition of a particular tube are suppressed, variations in the construction of one tube from another are not suppressed in this manner. The current drawn by the plate in this circuit will depend rather critically on the exact geometry of the elements of the tube, and in fact variations have been measured in new tubes of the order of two to one in the current drawn by the plate. Thus the condition (4a) is included to allow for such variations.

Condition (6) concerning the minimum number of tube elements appears at



first sight obvious, but its application is not always clear-cut. In its simplest form almost anyone would agree that with everything else equal the probability of failure of a circuit would in some manner increase with an increase in the number of elements included, both tube elements and also every other kind of element, resistors, condensers, tube sockets, and even wires. It also is reasonably clear from experience that tubes are in general more prone to failure than most of the other elements used in circuits - - - not only the cathode and heater, but also the other elements in the tube, supports, pins, and such. Because of the high temperature of the tube heater, the elements of tubes are working under more severe conditions than is common for other circuit components, and the pulling away of welds and similar failures have been observed repeatedly. In short, if a single triode will do the job there is no need to use a pentode, and on the other hand, if the choice were to lie between a single pentode and three or four triodes, it would be quite obvious that using the pentode would only be reasonable. However, if the particular circuits under consideration involved the alternative of either one pentode or else a pair of triodes, the question is not nearly so clear. On a simple count of elements the pentode would win unless the triodes could have a common cathode (such as the 6J6), but the final choice will probably lie either in the details of the rest of the circuit, or else in the designer's personal predilection.

Condition (11) has been included as a result of the experience with Shifting Register No. 1. There one of the two shifting pulses was applied to the circuit by pulsing the high-voltage end of the plate resistors of all the gate tubes. Whether the gates did or did not draw current during this operation

depended on the particular number being shifted; if the number was all zeros then none of the gate tubes functioned, while if it was all ones all of them functioned. Thus the load on the pulser differed with different information. Under such conditions there will be variations in the amplitude of the pulses reaching the circuit unless the pulser has a very low internal impedance. Experience with the register was that it was very difficult to get the impedance of the pulser low enough to avoid this kind of interaction.

Also in Shifting Register No. 1, the clearing pulse and the gating pulses were superposed, and applied to a common terminal. The clearing pulse was positive, and the gating pulse was negative and of greater amplitude. Provided a zero was being shifted from one state to the next, the gating pulse was inhibited and the clear pulse controlled the next stage. If, however, a one was being shifted, both the clear pulse and the gated pulse were applied, but the gating pulse being stronger overrode the clear pulse and produced a net negative pulse which set the succeeding toggle in the "one" position. Since the succeeding toggle was sensitive to pulses both positive and negative, it was necessary to be sure that the gated pulse completely overrode the clear pulse, without leaving any spurious signals of incorrect sign. Thus it was necessary to be sure that the gated pulse lasted until after the clear pulse had decayed, and it was necessary to control the time constants of the circuits through which the two pulses passed to be sure that under no condition would the clear pulse last until a later time than the gated pulse. These considerations resulted in the inclusion of criterion (8).

Sometimes additional circuit elegance may be achieved if pulses are distinguished according to their amplitude, say all pulses below a certain amplitude being rejected and all above that amplitude accepted. However, when it is

desired to push the operating speed of the equipment to as high a value as possible, it is necessary to use as short pulses as will operate the circuit, and under such conditions the time constants of the circuit reactions become of the same order of duration as the pulses. Under such situations the amplitude of the pulse actually reaching a circuit element is somewhat dependent on the exact time constants which exist, and accordingly discrimination according to amplitude requires much more careful attention to such time constants (and their constancy with age) than is necessary if this sort of discrimination is not used. Hence criterion (9).

Conditions (10) and (12) follow quite similarly, and indeed several of these criteria are but specific applications of criterion (7) that the individual parts of a circuit should be as nearly independent of each other as possible. This is believed to be good practice, not particularly because of any belief in the essential simplicity of nature, but rather because of the frequently observed essential simplicity of man. That is, it is useful particularly in improving the designer's understanding of the circuit and the ease with which troubles may be diagnosed.

A general thread will be noticed running throughout these criteria with respect to the accuracy which can be expected to be maintained by various circuit elements. In general, it is believed that tubes and crystal diodes should be expected to vary by a factor of 2 - - - - that is, either twice or one-half as good - - - while resistors are expected to hold their accuracy to as little as 10%. If it were particularly important for the realization of the circuit, a part of it would be designed with closer tolerances than those specified here, but under those conditions particular watch would be kept on such elements both



in testing and in maintenance to see that their accuracy is held. The use of such smaller accuracy limits would result in an increase in the frequency with which the circuit should have a maintenance checkup.

It will be noted that rather precise limits are given for the accuracy with which a voltage applied to the circuit from an external supply may be maintained. In the former circuit the number of voltages supplied from the outside was kept to a minimum, partly to keep down the number of contacts necessary in the plugs for each stage. When a voltage was needed different from the external supply it was developed within each stage by a resistor network. In the present design the former attempt to minimize the number of the supply voltages was abandoned because of the difficulty in maintaining accurate voltages with resistor-divider networks. It was felt that it was better to have one external supply whose voltage could be watched rather than a pair of resistors in each of the forty stages of the adder. Thus all critical voltages were supplied from regulated external supplies, it being evident that power supply voltages were capable of closer control than 40 individual dividers.

In this design, also, the first Kirchhoff summation was retained in view of its greater economy in tubes and components over binary gating schemes (see Progress Report No. 2, pg. 38), but the highly critical second summation was replaced with a modified binary gating system operating directly from the sum voltage of the first summation.

The new adder was designed as closely as possible in accordance with the principles described. Successive reference numbers were applied to successive designs, many of which were superceded before going into actual physical

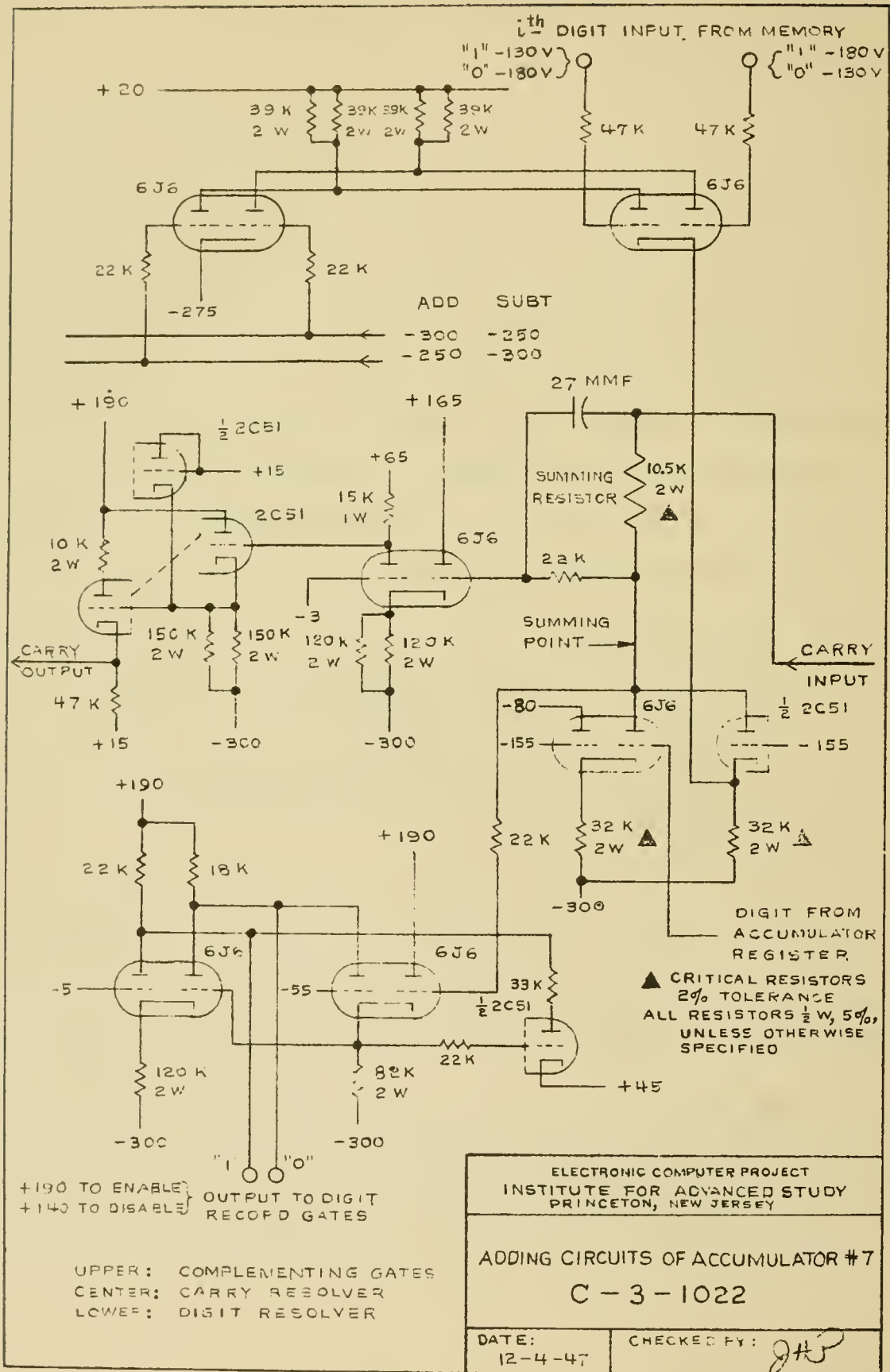
construction. Thus although the former circuit was known as No. 2, the next circuit to be built completely - - - and described here - - - is No. 7. The adding circuits are shown in Drawing C-3-1022. There it will be seen that the circuit is divided into three parts: the complementing gates, the carry resolver, and the digit resolvers; and it will be seen that the principle of keeping the different parts of a circuit as nearly as possible independent of each other has been carried out --- there is but a single connection between each part and the next.

As was done in Accumulator No. 2, the adder includes means for complementing the incoming number if desired. The complementing gates are so arranged that by proper manipulation of the Add-Subtract busses any of four possible input arrangements may be achieved:

1. The incident digit (I) itself may be applied to the adding circuits.
2. The complement of I may be applied; that is, if I is "0" the adder will receive the input "1", while if I is "1" the adder will receive "0".
3. The incident digit may be completely turned off; regardless of the value of I, the adder will receive only "0".
4. The input may be "1" regardless of the incident digit.

These results are achieved by the two tubes shown in the top of Drawing C-3-1022, together with the half tube at the extreme right of the center group. The incident digit is applied to the adding circuit in terms of a standardized current 4.5 ma, which comes from the plate of the 2C51 tube having its grid at -155 volts and its cathode returned to -300 volts through a resistor of 32K ohms. If this tube were not affected by the complementing gates, its plate would always produce this current whose value is determined almost entirely by





the voltage difference between -155 and -300 volts and the value of the 32K resistor. It is very nearly independent of the plate voltage and the tube characteristic; the circuit is so highly degenerative that the exact characteristic of the tube will affect the value of this current only to a very small degree. The complementing gates act under appropriate conditions to turn this current off by pulling the cathode of this standard-current tube above its grid potential. This is done by the upper right hand tube in the drawing, whose cathode is connected to the cathode of the 2C51. When this tube is drawing at least 4.5 ma it absorbs all of the current of the 32K resistor and none flows into the summing circuit. Thus the summing current is also independent of the exact characteristic of the complementing gates, provided only that they remain better than a certain minimum; no matter how strongly the complementing gates pull up on the cathode of the 2C51, provided only that they will pull with at least 4.5 ma, then the summing current is exactly zero.

In order to pull up the cathode of the 2C51, the digit information is applied to the grids of the upper right hand tube, having a potential either above or below the -155, depending on the value of the number applied. One grid receives a voltage which is high if the number is "1", while the other grid receives just the opposite, a voltage which is high if the number is "0". Then one or the other side of this tube is turned off by the upper left hand tube which when conducting reduces the plate potential of the right tube to below its cathode. Suppose, for example, that these gates are set to add. Then as indicated on the diagram the upper of the Add-Subtract busses is at -300 volts, while the lower bus is at -250 volts. Then the left side of the left tube is conducting and the right side is non-conducting. Consequently

on the right tube the left plate is below -155 volts while the right plate is above. This makes only the right side of the tube effective; on that side the grid is above -155 when I is "0" and below when I is "1". Accordingly this tube draws the cathode of the 2C51 up when I is "0", producing a summing current of zero, while when I is "1" the cathode of the 2C51 is not affected and the full summing current of 4.5 ma is applied.

When the busses are set for subtraction the opposite side of each of these gates is in operation and accordingly the number I is complemented in developing the summing current. For some applications it is desirable to turn off the input I, regardless of the value of I. This is readily accomplished by putting both of the Add-Subtract busses at -300 volts, when both sides of the complementing gates are operative, and since one grid or the other is high in potential no matter what the value of I, the summing current is zero. Similarly if it is desired to apply the input "1" regardless of the value of I it is merely necessary to set the busses at -250 volts, when both sides of the right hand tube are inactive and the summing current is at its full value of 4.5 ma.

As was done in Accumulator No. 2, the actual summation is done by the superposition of standardized currents and voltages in a resistor network (called "Kirchhoff summation"). To provide for speeding up the propagation of a carry from one stage to the next (at the expense of the speed of input to a particular stage), the standardized inputs consist of two standard currents and one standard voltage. The two standard currents, representing the incident digit, I, and the resident digit, R, are each of 4.5 ma and are applied to the bottom of the 10.5K summing resistor. Thus each of these currents produces a voltage drop across this resistor of about 50 volts. The third input is

that of the carry coming from the preceding stage. It comes from a cathode follower which supplies a voltage of about +70 volts for a "0" and +20 volts for a "1" (The voltages supplied to the circuit are actually +15 and +65 volts; which allows for the difference in potential between the grid and cathode of the cathode followers). This cathode follower voltage is essentially independent of the value of the two summing currents applied (Actually the slight dependence of the cathode follower output voltage on the current drawn by the other two inputs is included as part of the design. The cathode follower presents an output impedance of the order of 500 ohms. Accordingly the summing resistor has been made that much smaller than its theoretical value of 11K; so the real summing resistance is the 10.5K resistor in series with the 0.5K internal resistance of the cathode follower). So the applied voltage of the carry and the two applied currents of the other digits have equal effect on the summation voltage; it changes by 50 volts for each additional input. The voltages at the summing point are:

No. of incoming "1"s		Summing point voltage
Decimal Notation	Binary Notation	
0	00	+70
1	01	+20
2	10	-30
3	11	-80



One way in which reliability has been increased by the new design is obvious from the comparison of this table with the one for Accumulator No. 2 — the voltage differences have been made just twice as large, so that the variation of components will produce less effect. It might be mentioned that such variations entering into the value of the summation currents or voltage, would here have just as bad an effect as in the former case, the whole effect here just being scaled up from there, but on the other hand here the gate voltages which are going to split this sum up again into a binary representation need not be so carefully controlled.

We have already described the manner in which the standardized current representing the incident digit, I, is applied to the summing resistor. The digit from the accumulator resistor (Resident digit, R) is applied in the same way, except that here no provision is made for complementing. This function is performed by the 6J6 directly below the summing resistor on the diagram.

The carry is sensed by the 6J6 whose grid is connected to the summing point through a 22K resistor. The two sides of this tube are coupled by the common cathode resistor, and since the other grid of the 6J6 is connected to -3 volts, whenever the voltage of the summing point is below this value the cathode current will flow to the left-hand plate of the 6J6, but any summing point voltage above the -3 volts will cause the cathode current to flow to the right-hand plate. Accordingly the current flows in the left-hand plate only when the inputs are appropriate to produce a carry; that is, when the inputs to this stage of the adder consist of two or more than two digits. The left-hand plate of this 6J6 gate tube is connected to two cathode followers in series which act as current amplifiers so that the carry voltage sent on to the next



stage will be relatively independent of any current which may be drawn from the output. Between the two cathode followers is a tube connected as a diode, which prevents the carry voltage from swinging below its appropriate lower value of +15 volts. Thus the carry voltage is standardized at both its limits; the upper limit of +65 volts occurs when there is no voltage drop across the 15K plate resistor, and so is determined by the external supply of +65 volts; the lower value is determined by the diode which limits at +15 volts.

There are several features of this design which contribute to the speed of the carry propagation from one stage to the next. One of these is the use of two cathode followers in series. Had a single one been used large enough to carry the output load its capacity applied to the plate of the gate tube would have slowed up the circuits. Detailed calculation has shown that a cathode follower introduces only a very small delay in the propagation of a signal provided the maximum rate of change it can produce in its cathode is at all greater than the rate of change of the signal. Also the current requirements on the output are such that in order to supply them with the reliability required by our design criteria it is necessary to permit this second cathode follower to draw grid current at times. This grid current is supplied by the first cathode follower where it couldn't have been supplied from the plate load of the gate tube without producing inaccuracy.

Similarly, the diode is placed between the cathode followers rather than directly on the plate of the gate tube because in the latter location its capacity would limit the carry speed.

Another feature of the design which speeds up the carry is the inclusion of the 22K resistor between the summing point and the grid of the gate tube, together with the 27 mmf condenser from the carry input to the gate tube grid. This circuit introduces a time delay in the propagation of a signal from the summing point to the gate grid, since if either R or I is changed, the voltage change they produce on the summing point must charge the 27 mmf condenser through the 22K resistor. On the other hand, a voltage change produced on the carry input is coupled directly to the gate grid through the condenser and so can change the gate operation even though the plates of the tubes supplying the R and I current have sufficient capacity that it takes an appreciable time for this voltage change to reach the summing point. This whole procedure is a reliable one because whenever a voltage change appears on the carry input that entire voltage is supposed to reach the carry gate grid; this connection serves merely to speed up the carry input at the expense of the other two inputs. This will, of course, cause delay in the starting of a carry in the first few stages after it starts, but with a possible 40 stages for it to propagate, the gain in speed in the later stages far overshadows the loss in the first few. Indeed a small speed improvement would result from omitting these elements in the first few right-hand stages.

In Accumulator No. 2, the information concerning the resultant digit for each stage was obtained by subtracting from the voltage of the summing point an additional voltage dependent on whether or not a carry was produced by the stage in question. This resulted in an undesirable accumulation of errors, so in this circuit the resultant digit information is generated by a

straightforward gating technique, using the voltage at the summing point as the input to the digit resolver gates.

Since there are three inputs to each stage, ---R, I, and C --- there are four possible sums --- 0,1,2, and 3. At first it would appear as though the digit resolver circuit should given an input to the recording gates which will impress the appropriate value on the accumulator register for each of these four sums. It turns out, however, that in two of the four cases the toggle of the accumulator register is already in the correct state and does not need to be changed. The possible values are:

Number of inputs		Summing Point Voltage	New Resident Digit R'	Old Resident Digit (R) Known To Be:
Decimal Notation	Binary Notation			
0	00	70	0	0
1	01	20	1	?
2	10	-30	0	?
3	11	-80	1	1

When the sum at the summing point is zero, it is obvious that each of the three inputs is itself zero. Thus we know that the Accumulator Register Toggle R is in state zero, and it is to be put in state zero. Similarly, when the sum is three, the Accumulator register toggle must be in the state one and it is to be left in the same state, so there is no need to make any change in it. Accordingly in these two cases the digit resolving gates give no output to the recording gates, and the recording gates are disabled so that when they are pulsed they will make no change in the accumulator toggle.

In the other two cases, however, when the sum is either one or two, the appropriate recording gate is enabled to record respectively a one or a zero.

Thus although the recording gates are inactive in certain instances when the accumulator toggle does not need to be changed, this is not generally true. If the sum is either one or two, the accumulator toggle could be in the right position not to need changing, but it could also be in the other position; the resolving circuit does not know and so impresses on the toggle the correct state whether or not it already is in that state.

For the two cases where the digit resolver circuit does have an output, it is generated by two gate tubes having a common plate load. For the "0" output, one of these plates draws current when the sum is 0 or 1, while the other draws current when the sum is 3. Thus the output is high only when the sum is 2, which is the condition under which a "0" is to be recorded.

Without going into details of the numerical results, let it suffice here to say that the operation of each portion of the circuit was calculated with allowance for the variations stated in the design criteria. The results quoted previously for the shifting register design have shown the application of such calculations to a much simpler system. The adder ---- even including the Kirchhoff summation and gating --- was calculated to be stable under such variations, and in addition the speed of carry propagation was studied with considerable care and made as fast as seemed feasible within the design criteria.

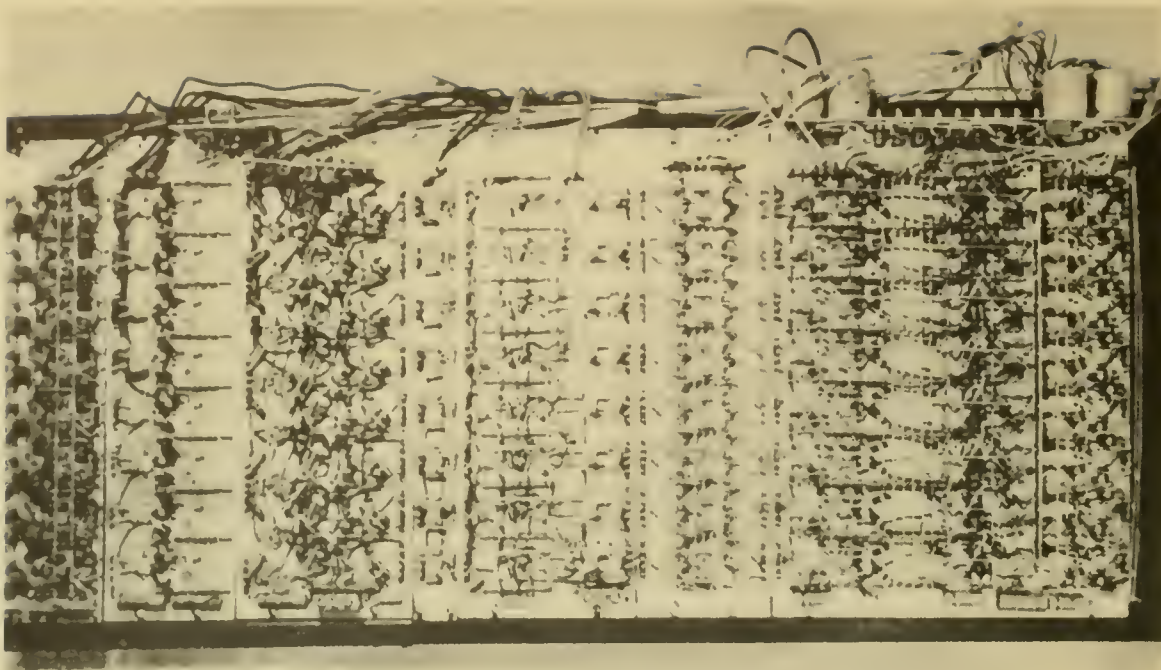
Eight stages of this new adder design were laid out and built, using checked 5% resistors. In distinction to the previous practice of separating



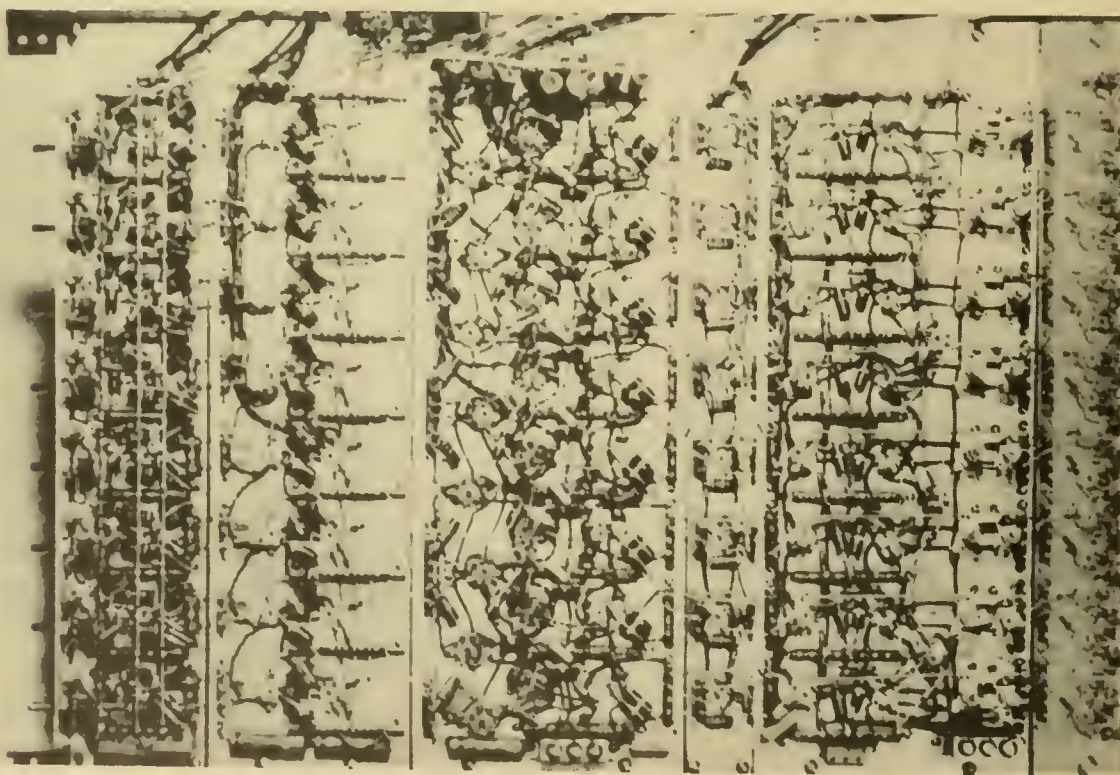
chasses by digits, the new adder was laid out in function strips; that is, 8 stages of complement gates were built on one chassis, 8 carry resolving stages on another, and 8 digit-resolving stages on yet another. The number 8 was chosen as a convenient submultiple of 40 and with regard to mounting in a standard 19" relay rack with a 2" spacing between stages. An 8-stage toggle strip, with individual switches to set to "0" or "1" was constructed to simulate the incoming digits from the memory register and the whole assembled on a table-size relay rack. (See Photograph 5b) All necessary power supplies were assembled in a large relay rack and provided with master heater and plate switches and individual voltmeters, so that all power to the adder could be controlled by one switch. Some of the lower voltages are supplied from batteries and these are also metered and controlled on the rack. All critical voltages are furnished by either regulated supplies or storage batteries. Quite aside from mere convenience of operation, the use of a common control for all plate voltages is particularly desirable to avoid the possibility that some circuit elements may be overloaded in the process of turning the various power voltages on and off one by one. With such wide differences in d.c. voltages as appear in this circuit this is particularly true of heater-cathode potentials; these potentials are designed to lie within the allowed range when all voltages are applied, but particularly in circuits with cathode resistors returning to large negative voltages there is a possibility that excessive heater-cathode voltage would appear should the voltages be turned on at different times.

When the adder was first energized, one tube (2C51) although from new stock, was found to have a heater-cathode short. When this was replaced, the adder functioned without need for any circuit adjustments.



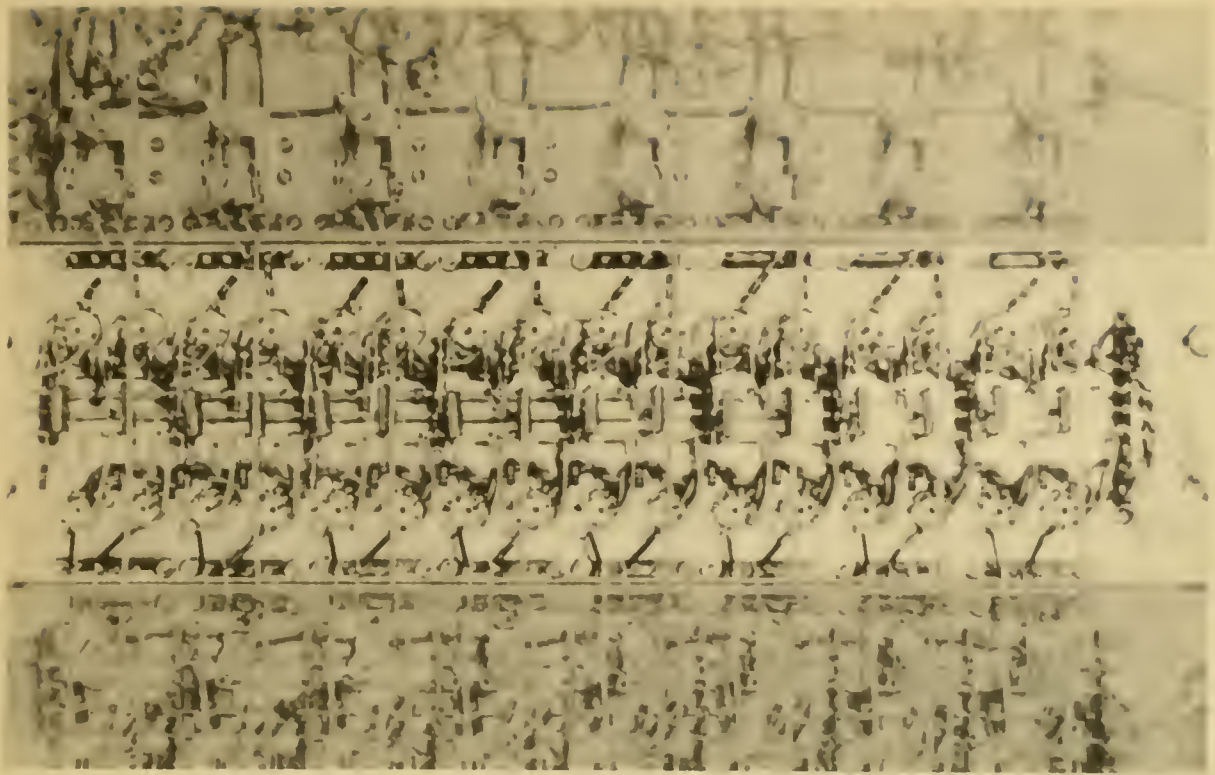


Photograph 5a. Accumulator No. 7, complete unit.

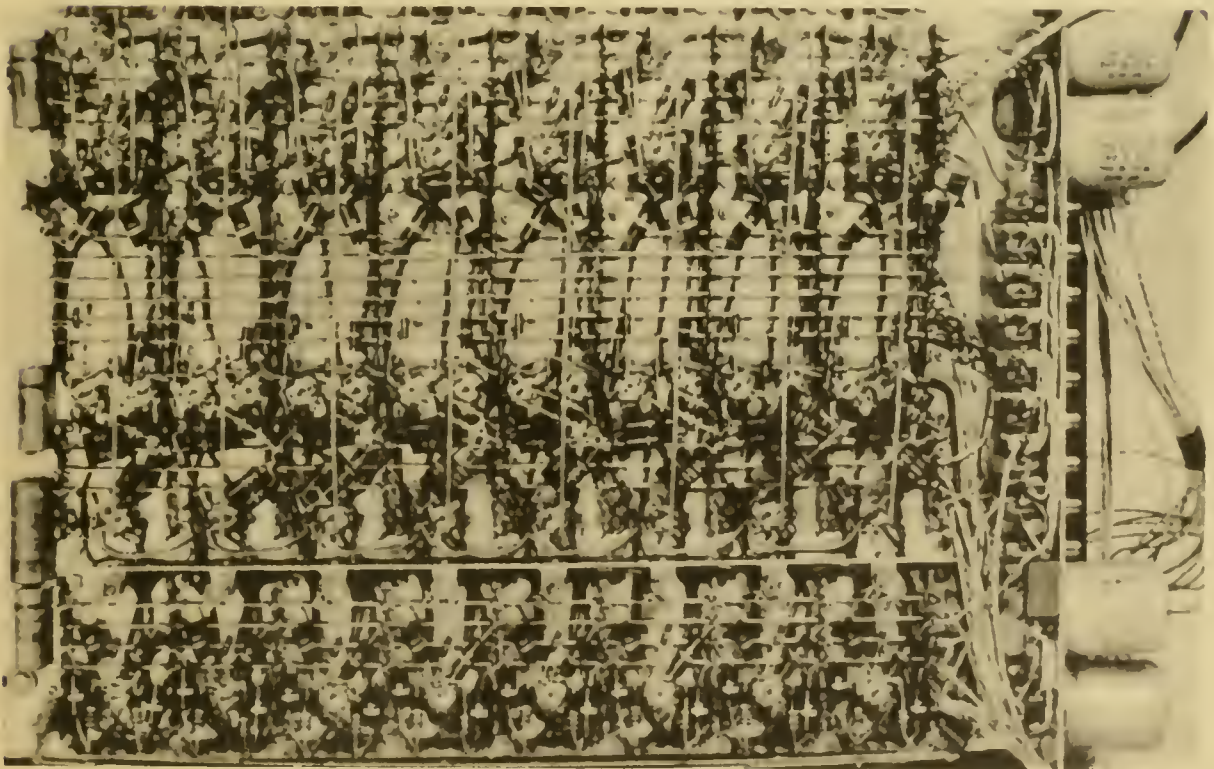


Photograph 5b. Accumulator No. 7, adding circuits.





Photograph 5c. Accumulator No. 7, digit recording gates.



Photograph 5d. Accumulator No. 7, shifting register.

All electrode voltages in each stage were measured and found remarkably uniform from stage to stage, reflecting the close design control and the elimination of off (5%) tolerance resistors prior to installation. New stock tubes were used without selection.

Carry-speed measurements were made by dynamically introducing and removing the "artificial" carry into the extreme right stage and measuring the rate of propagation of the carry along the stages. A per-stage carry time of 0.14 microseconds was observed, corresponding to a 40-digit carry time of 5.7 microseconds.

The adding circuit was designed to maximize stage-to-stage carry speed. If a carry is generated by complementing an incident number consisting of all "0"s, that is, suddenly impressing all "1"s on the input, the carry from the first stage (but not succeeding stages) requires between 1.5 and 3.1 microseconds to propagate to the next stage, the extra delay being due to the speed maximizing elements mentioned above. In the 8-stage adder this extra delay is comparable with the time saved in 8 stage to stage carries; in a 40-digit adder it would be small. Summarized, the carry time appears as follows:

Basic propagate time for 40 stages . . . . .	5.7 microseconds
Extra time needed for carry to attain above speed (in early stages) . . . . .	3.1       "
Digit output response time from reception of carry into last stage . . . . .	<u>1.5       "</u>
Total carry time . . . . .	10.3 microseconds

To this time must be added the time taken to impress the incident number, a function of the memory; and the time taken to gate the new R' into the desired position in the register, a function of the recording gates and the register.

The effects of varying supply voltages were studied. Carry time was found to depend directly on some of the critical voltages, as was expected; however, no trouble was experienced in maintaining these voltages. Heater voltages on all tubes, nominally 6.3 v, were reduced to check the circuit performance under low emission conditions (see previously). Proper operation was obtained down to 4.0 volts and carry speed showed a slight increase.

Studies were made of several ways to increase carry speed, such as increasing carry cathode-follower currents and decreasing the carry-gate plate resistor. While these measures showed promise no changes are being made at present, since the carry speed is probably already adequate. Circuit capacities were measured at critical points, time constants computed, and the experimentally determined response times verified by calculation.

This adder has been in operation for many hours each day since it was first energized on 22 October and has developed no trouble except for a tube failure (heater-cathode short).

b. Recording Gates No. 1 The digit inputs to adder No. 7 are at a negative voltage level (-155) but as the information is passed through the circuits in the adder the accumulated grid-to-plate voltage rises result in a digit output level at +140 to +190 volts. This step-up of levels is common to all d.c.-coupled adders so far discussed. In the Accumulator No. 2 design (see IV B 1 c) a special d.c. translation circuit was used, in addition to various condenser couplings, in order to compensate for this rise and reduce the output level of the carry to one suitable for presentation at the input of



the next stage. In Adder No. 7, the carry process is so designed as to need no explicit translation, but the digit output information ( + 190 level for "1"s) must be gated into the accumulator register, which is at the input level of -155 volts.

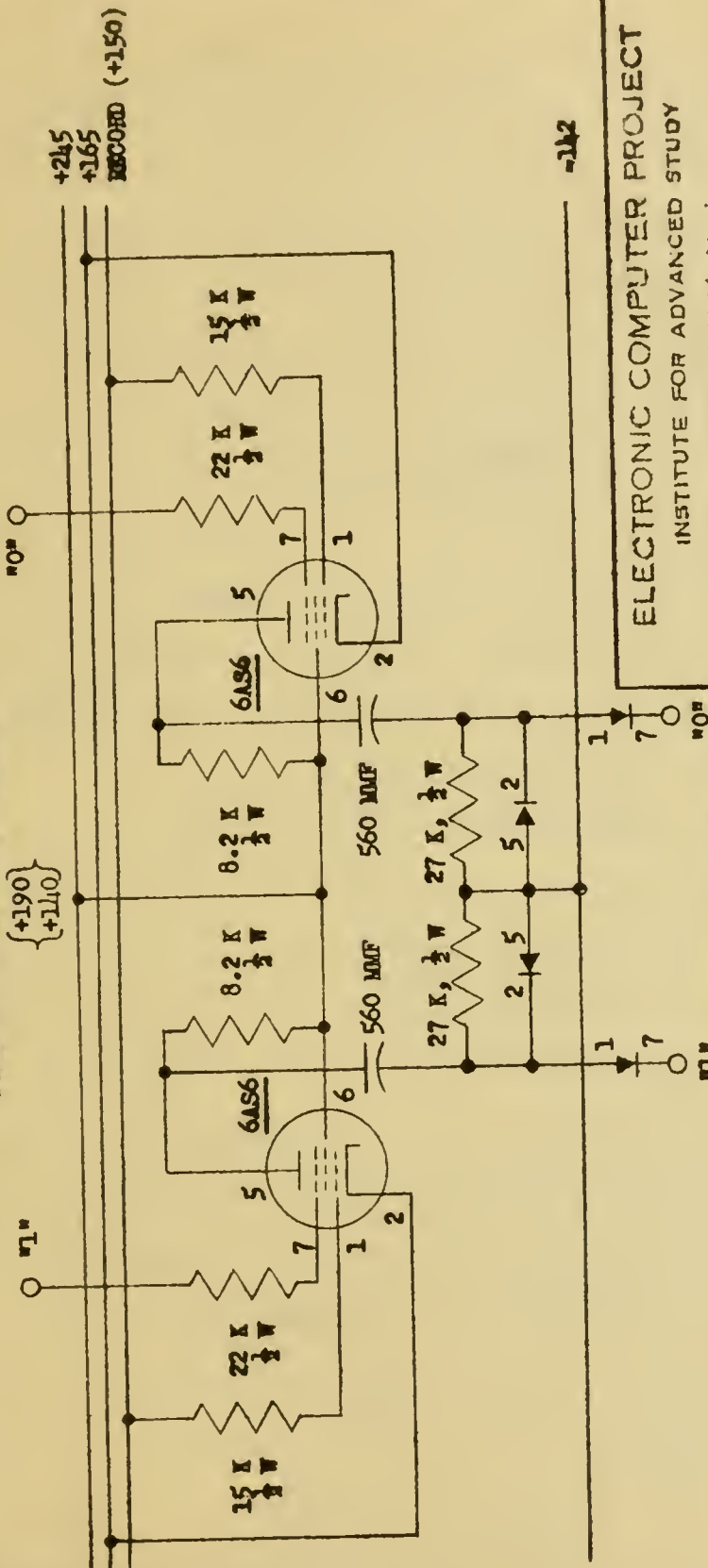
Since the operation of recording the output digit cannot be a continuous operation, it is convenient to transmit the digit information down by gated pulses, with blocking condensers in series to isolate the d.c. levels.

Gating of the digit pulsers is accomplished with the 6AS6 double-control-element gate (see Drawing C-3-1025). The design criteria enumerated in the previous section are adhered to.

The operation of the gates is quite straightforward. The digit resolving chassis provides on both the "1" and the "0" output either +190 volts to enable the gate or +140 to disable it. (Note that the +190 enabling voltage is equal to a supply voltage, being derived from a cut-off plate, and can therefore be closely maintained). The enabling voltage is applied to grid #3 (pin 7) of the 6AS6 through 22K resistors to limit the "on" current to about 1 ma. The cathode (pin 2) is connected to the +165 bus so that the grid #3 supply voltage is either +25 or -25 with respect to it. When grid #1 (pin 1), which is normally sufficiently negative to completely cut off the space current, is pulsed positively, either a large plate and small screen (grid #2) current will flow if grid #3 is 0 or a few volts positive with respect to cathode (+190 from the digit resolver), or zero plate and a large screen current will flow if grid #3 is negative with respect to cathode (+140 from digit resolver). The 6AS6 plates (pin 5) are coupled to the proper register toggle grids through 560 micro-microfarad condensers.



FROM DIGIT RESOLVING CHASSIS



ELECTRONIC COMPUTER PROJECT  
INSTITUTE FOR ADVANCED STUDY  
PRINCETON, N. J.

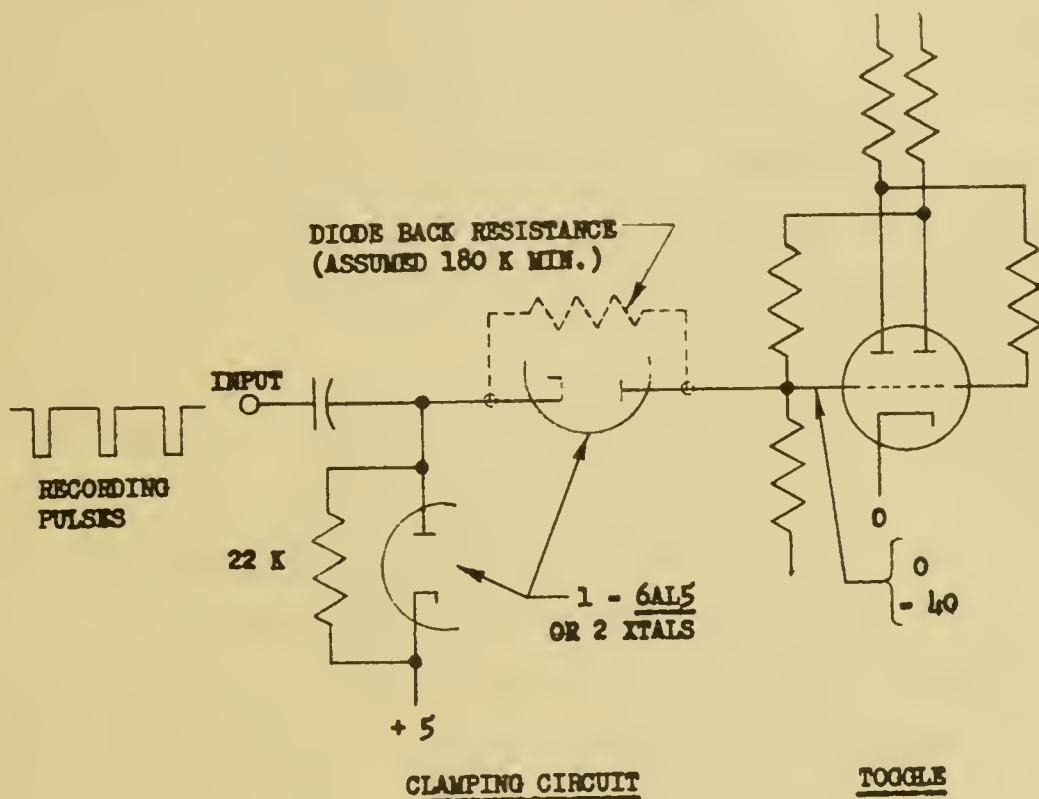
DIGIT RECORDING GATES NO. 1

C - 3 - 1025

DATE	DRAWN BY	CHECKED BY
12 - 15 - 47	H. HART	J. H. R.

Notice that here no d.c. translation is used; a blocking condenser is used to separate the disparate levels and the digit information is transmitted through it as a negative pulse. Since no d.c. information is transmitted, the average voltage on the toggle grid will remain constant. This means that unless corrective measures are taken, the baseline or dwell between the negative pulses will shift positively as the pulsing duty factor increases: for example, a 0.25 microsecond pulse applied once every microsecond will result in a shift of toggle grid voltage (between pulses) of  $\frac{1}{4}$  of the pulse height or +10 volts for a 40-volt signal. This voltage shift resulting from the loss of the d.c. information is familiar in television work, where it is corrected for by a shunt clamping or "d.c.-reinsertion" diode; the situation is complicated here by the toggle grid's having not one but two possible reference levels neither of which must be permitted to shift.

The problem is solved by a shunt and series diode combination (see Drawing C-3-1027), of which the design considerations are of some interest. If the toggle grid swings between 0 (on) and -40 (off), the shunt diode can be returned to 0 to prevent a voltage shift above 0. The series diode is added to disconnect the clamping point from the toggle grid for the -40 case. If the toggle grid were to dwell in this state for a considerable period, the clamping point would tend to discharge toward -40 through the back resistance of the series diode so that it would eventually reach some value between 0 and -40 as determined by the relative back resistances of the two diodes. A subsequent command (from another driving point) for this toggle to change its state back



ELECTRONIC COMPUTER PROJECT  
INSTITUTE FOR ADVANCED STUDY  
PRINCETON, N. J.

CLAMPING CIRCUIT FOR PULSED TOGGLE GRID

C - 3 - 1027

DATE

12 - 19 - 47

DRAWN BY

H.H.

CHECKED BY

HP

INITIAL

again would require this grid to rise from -40 volts to 0 volts, but when it reached the voltage to which the clamping point had settled, it would find itself loaded by the gate plate impedance through the series diode (since it is now conducting). This would very seriously affect the toggling speed, but the possibility is avoided by returning the shunt diode to +5 volts rather than 0 and paralleling it with a 22K resistor so that the voltage divider consisting of it and the back resistance of the series diode (assumed 180 K minimum) produces an equilibrium clamping-point voltage not less than 0 when the toggle grid is at -40. Thus the toggle grid will at no time be loaded by the clamping circuits.

c. Register For use with this adder in forming a complete accumulator. Register No. 3 has been assembled and connected to it. A picture of the complete assembly is shown in Photographs 5a, and in Photographs 5c and 5d are shown details of the digit recording gates and of the shifting register. This combined assembly has just been completed and detailed pulse tests of the operation of the entire accumulator have not been finished. However, addition, subtraction, and multiplication have been carried out by manual control, and preliminary pulse tests have been made of the speed of addition and recording into the register. These preliminary tests are in good agreement with the data measured on the adder and register separately.



## V. CONTROL ORGANS

While the arithmetic organs are capable of carrying out all of the numerical operations of the machine, they need a highly complex grouping of pulses applied to them to perform these functions. It is a debatable point where the dividing line should be drawn between arithmetic and control organs. One might, for instance, consider that all of the circuits necessary to carry out a multiplication belong to the arithmetic unit rather than the control. However, because of the similarity between the problem of constructing a circuit which will produce the appropriate sequence of pulses to perform a multiplication and the problem of constructing devices to locate the appropriate orders in sequence and interpret them for the rest of the machine, we have chosen to include all of these features in the general heading of "Control." The exact nature of the control circuits is strongly affected by the form of the arithmetic organs, and it is only recently that the arithmetic organs have been sufficiently advanced to make the consideration of the control either necessary or reasonable. Thus our work on this subject is just starting intensively and is expected to be the major problem of the coming months.

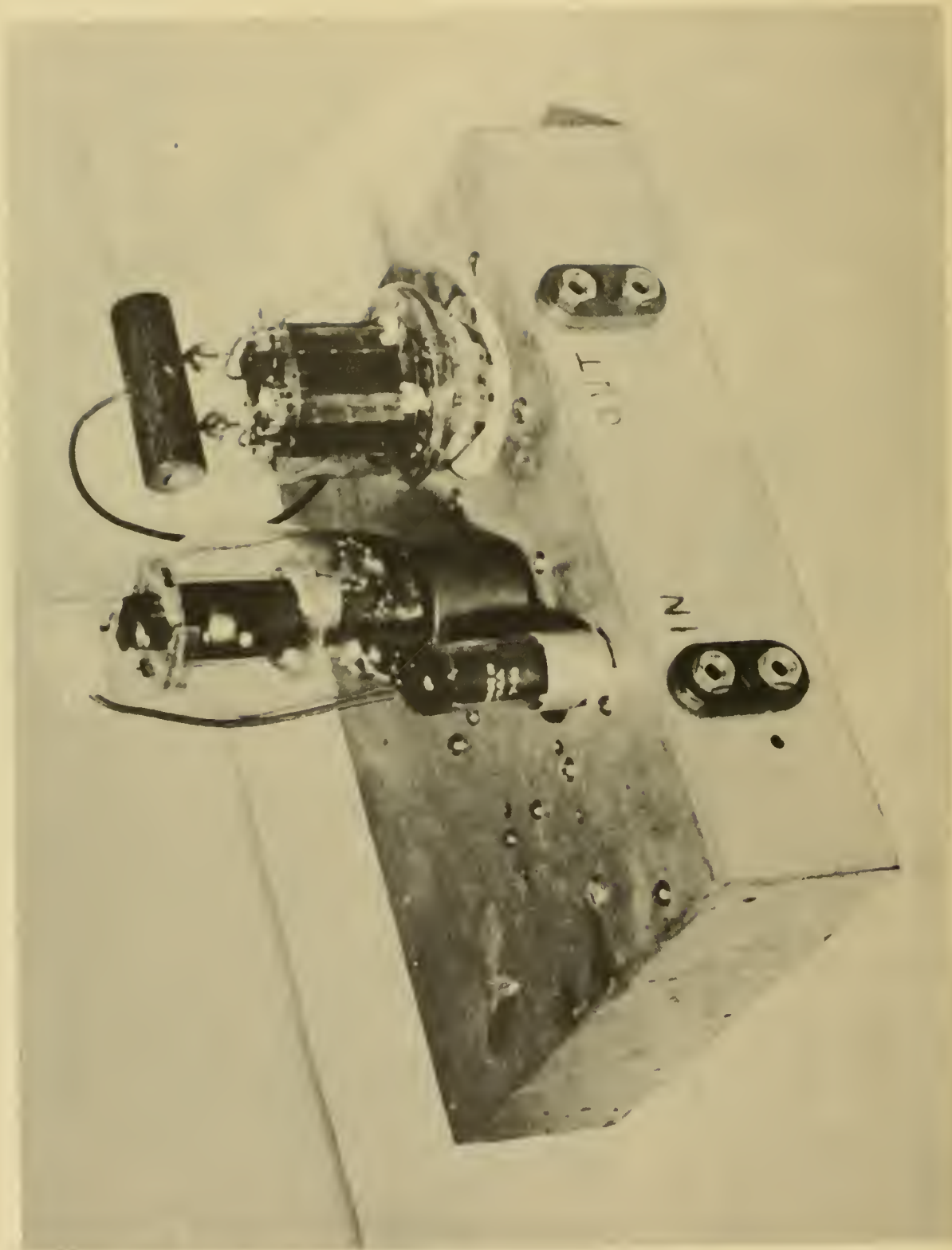
Work has been done on some of the component parts; pulses and binary counters and a multiplier circuit (for positive numbers only) were constructed to work with an early form of the accumulator. These are reported here.

## A. PULSERS

### 1. Pulser No. 1

For use with the Multiplier No. 1, a prototype trigger tube, blocking oscillator, and power-output cathode follower were constructed and tested. The schematic diagram of this unit is shown in Drawing C-3-1026 and its physical appearance in Photograph 6. Basically the circuit consists of a blocking oscillator (Type 807) which is triggered in the cathode by the trigger tube (6AQ5) and which delivers an output pulse also from the cathode to the output cathode follower (3E29, both sections). The blocking oscillator is connected in usual fashion to the transformer whose polarity is such that a negative plate signal produces a positive grid signal. The other end of the grid winding is returned through a resistor to a bias source and also through a capacitor, which determines the output pulse width, to an a.c. ground (true ground or the bias source); the free end of the plate winding goes to B-plus, in this case 800 volts. The screen of the 807 is supplied from 400 volts and a 270 ohm cathode resistor supplies the output pulse. This same cathode resistor also serves as the a.c. plate load of the trigger tube which stands normally cut-off. A positive pulse on the trigger grid produces a negative pulse on the blocking oscillator cathode which is equivalent to a positive grid pulse and starts the flow of plate current. This negative position of the blocking oscillator cathode pulse is rejected by the cut-off cathode follower. Because of the close coupling through the transformer, there results a positive grid signal which regenerates the action. The tube current continues to increase until anode saturation is reached at which point the tube continues to operate until the grid capacitor





Photograph 6. Pulser No. 1.



can no longer supply the current requirements of the grid. Then the grid voltage begins to fall, and by transformer coupling the rising plate voltage enhances this fall. The large tube current (of the order of 1 ampere for this oscillator) produces a positive output pulse at the cathode of the order of 250 volts. When taking output from the cathode of a blocking oscillator it is necessary to run the plate (and screen) at a sufficiently positive voltage that these two elements still have an adequately positive supply when the cathode rises to the peak pulse voltage. In order to produce the short pulses required (0.08 to 0.10 microseconds) a special transformer was constructed of four small Hypersil cores arranged along two perpendicular diameters of a circle to form a torroidal shell. This allowed an increase of fourfold in the core area without a series increase in the winding length of the coils. This increase of core area was necessary to avoid saturation at such high currents. Relatively small coils (15 turns and 20 turns respectively for the grid and plate windings) were used in order to keep the necessary stray capacities low. The pulse output with this arrangement was essentially rectangular although the flat top of the pulse was only approximately  $1/3$  of the total pulse width. The maximum repetition rate is determined except for tube dissipation by circuit recovery time and in this design was of the order of 0.6 microseconds. It was therefore necessary to assure that the trigger was always narrower than 0.6 microseconds.

The power-output cathode follower consists of both sections of a 3E29 beam tetrode working into a 20 ohm cathode load. A pulse of the order of 150 volts was developed across this load indicating a peak pulse current of the order of 7.5 amperes. With these currents it is very essential to have large capacitors close to the plates of the tubes to supply this instantaneous

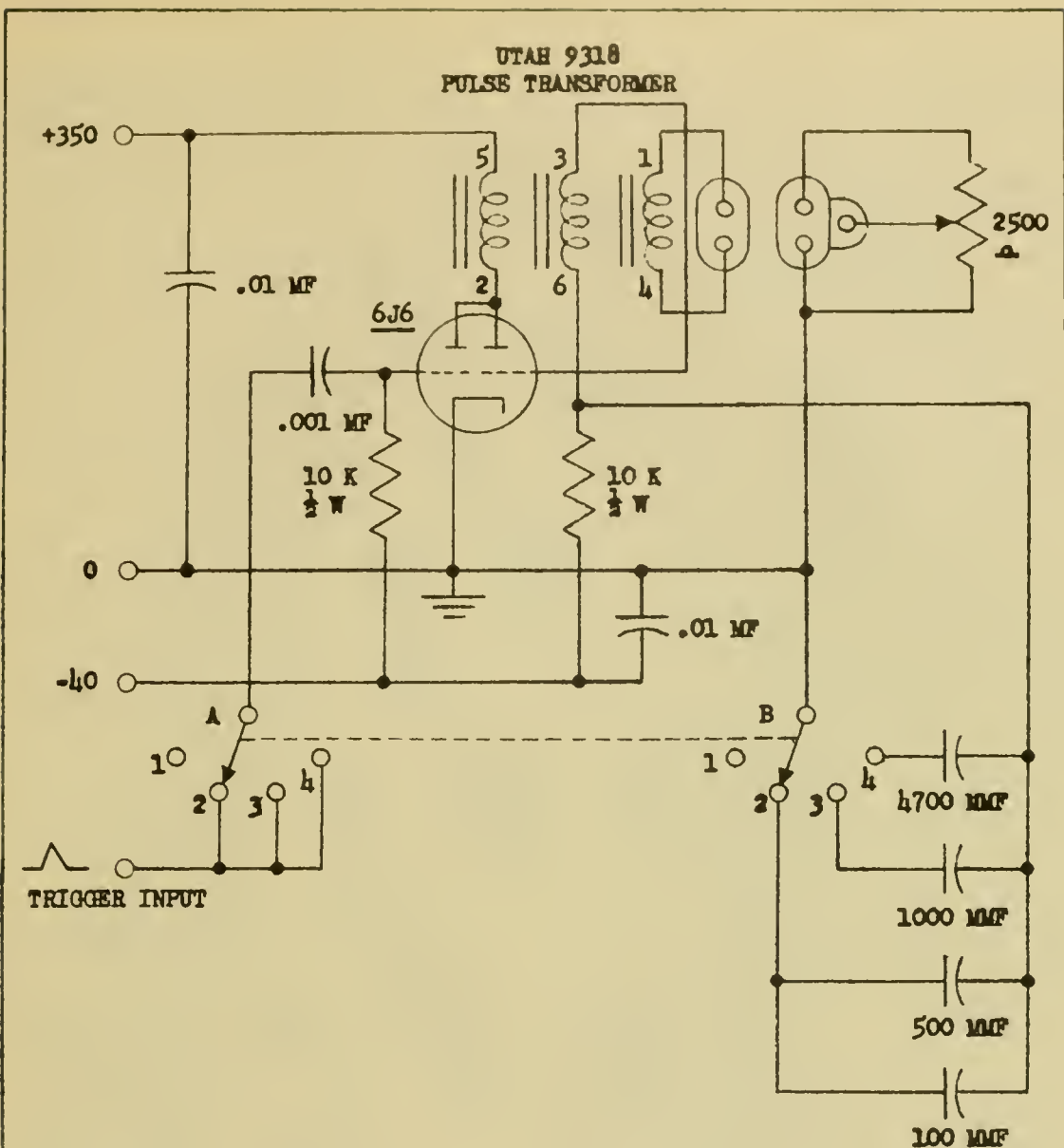
demand. This low output impedance was necessary for a number of reasons: (1) a substantial capacity load had to be driven; (2) good regulation was necessary for driving the clear busses of the arithmetic organs; (3) it was necessary to keep the common impedance between adjacent stages of the arithmetic organs to a minimum. These last two points have been discussed in more detail in section IV.

## 2. Pulser No. 2

Limitations in the decay of pulses from the laboratory four-stage sliding pulser apparently determined the minimum register-shifting speed. It was decided to convert the sawtooth pulser waveform into an essentially rectangular pulse by driving a blocking oscillator. The schematic is given in Drawing C-3-1024. A chassis containing four identical blocking oscillators was attached to the top of the four-stage sliding pulser. (see Photograph 7.)

With the selector switch in position 1, no trigger is fed from the 6D4 discharge tube, and the blocking oscillator does not function. This was included so that the 6D4 could be unloaded when its sawtooth was used directly. In position 2 the switch produces an approximately rectangular pulse at terminals 1 - 4 of the pulsetransformer with a rise time of about 0.1 microseconds and a width of 0.3 microseconds. The unloaded amplitude is 225 volts, and represents the amplitude of the plate swing, since the transformer winding ratio is 1 : 1 : 1.

As a convenient control of amplitude a 2500 ohm potentiometer was connected to terminals adjacent to the transformer output. When loaded with this potentiometer, the tertiary winding delivers a pulse of 150 volts amplitude. Either positive or negative polarity is available, being determined by grounding of the appropriate terminal.



# ELECTRONIC COMPUTER PROJECT

INSTITUTE FOR ADVANCED STUDY

PRINCETON, N. J.

PULSER NO. 2  
BLOCKING OSCILLATOR

C - 3 - 1024

DATE

12 - 9 - 47

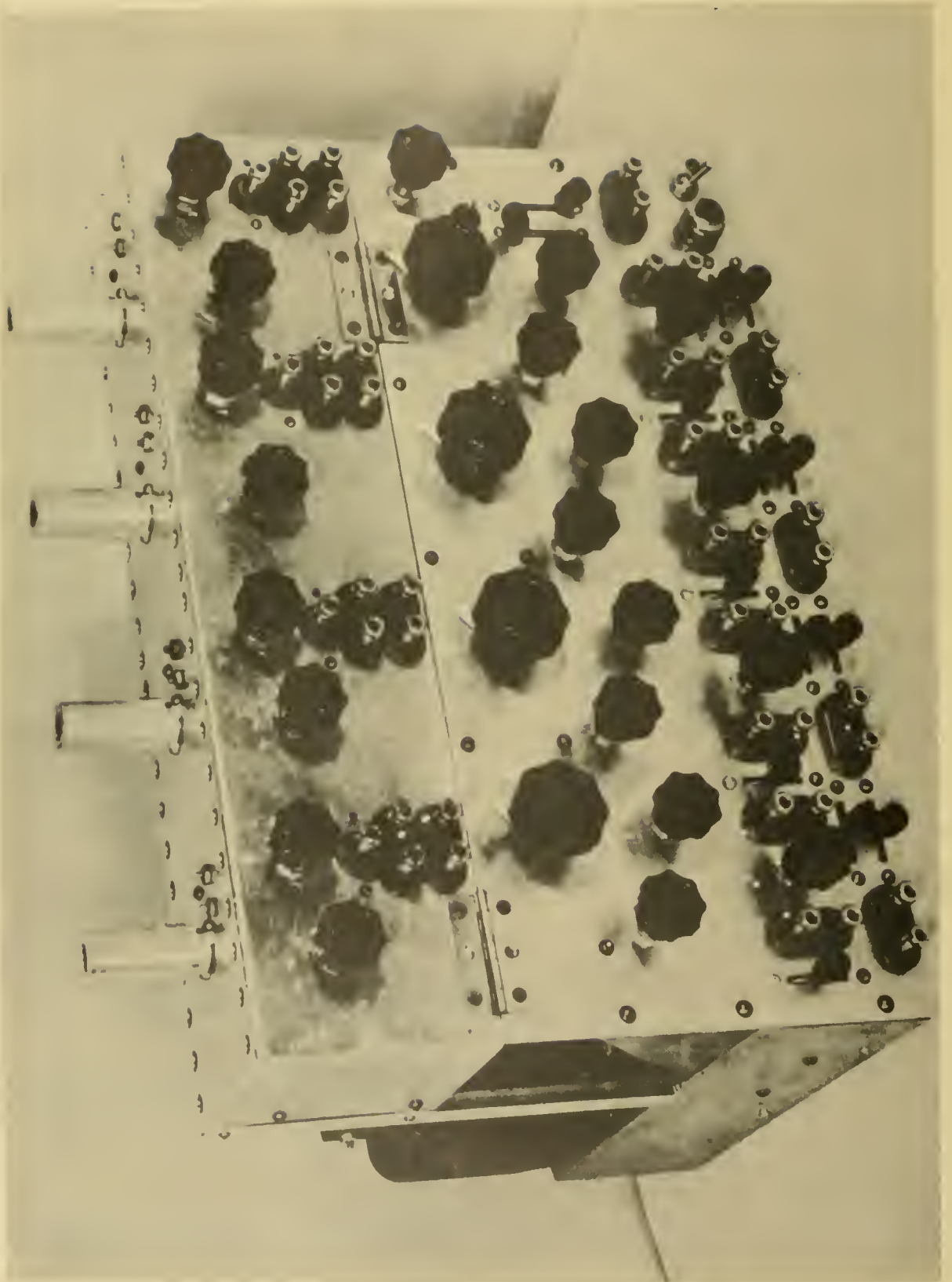
DRAWN BY

H. HART

CHECKED BY

*JR*

INITIAL



Photograph 7. Pulser No. 2 attached to quadruple variable pulser.



Switch position 3 produces a pulse width of 0.5 microseconds, and position 4 one of 0.7 microseconds width. The width is controlled by the recovery time constant of the grid return circuit of the oscillator tube. In an experimental model an 0.01 microfarad condenser in this circuit produced a fairly rectangular pulse of 1.5 microseconds width. This was not included since the switch had only four independent positions, and 1.5 microseconds was considered too wide for register work. Typical pulse shapes are shown in Drawing C-3-1035.

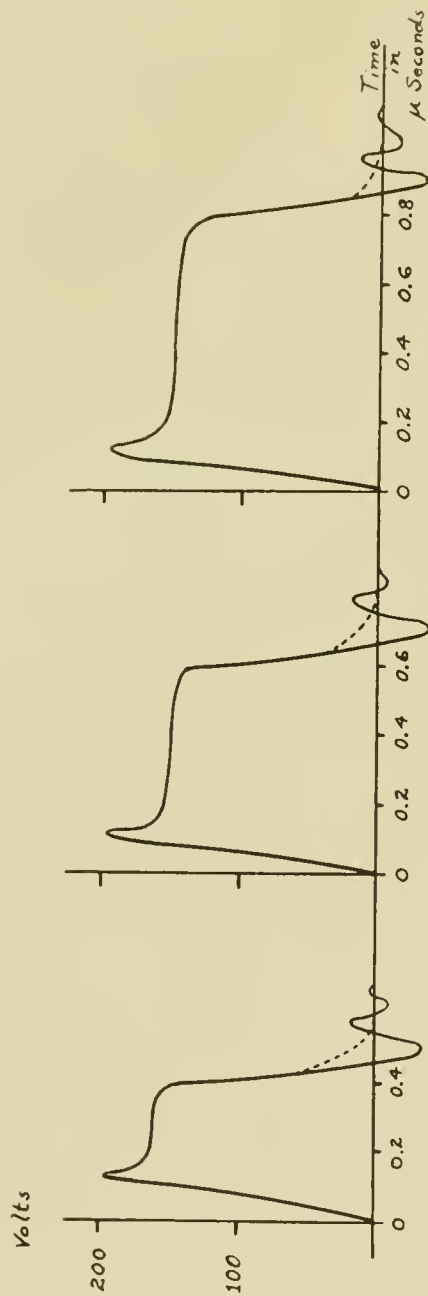
The positive overshoot at the initiation of the output pulse is due to the input trigger feeding through, and can be varied by controlling the amplitude of input trigger. It is usually found desirable to establish a compromise between fast rise-time and minimum overshoot. For a 0.1 microsecond rise-time the overshoot amounts to approximately 40 volts.

Pulse widths for the four similar stages constructed were quite uniform. Normal deviation was  $\pm 0.05$  microseconds, except that the maximum width of one oscillator was 0.6 microseconds instead of 0.7 microseconds. Components were installed unselected, so it is likely that the deviation results from variation in capacitance.

## B. COUNTERS

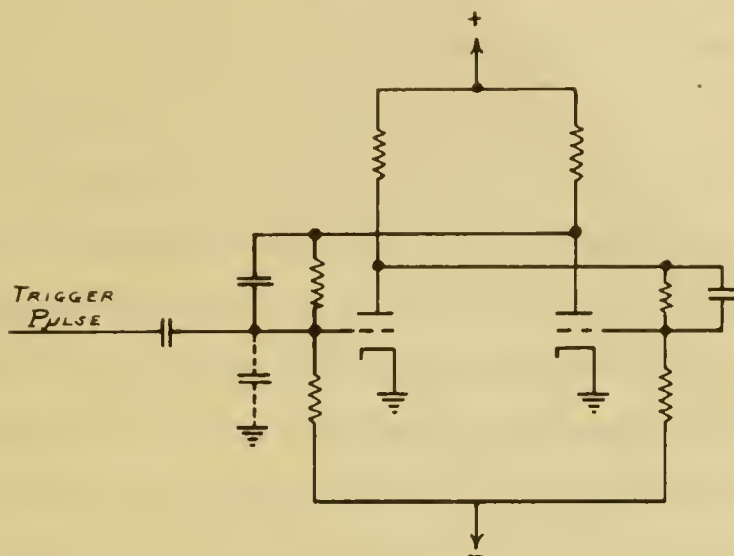
As a preliminary to the discussion of the counters, and as an aid to understanding some of the problems that arise, it is advantageous to discuss the various methods of triggering the toggle circuit and to state the restrictions which accompany each method.

Consider the conventional Eccles-Jordan type circuit with capacitors shunting the transpose (plate-to-opposite-grid) resistors. (see drawing C-3-1041). This circuit if properly designed will have two stable d.c. states, and will if pulsed properly, alternate between these states.



----- = Negative offshoot eliminated with IN 34

ELECTRONIC COMPUTER PROJECT Institute for Advanced Study Princeton, N.J.	
PULSES FROM PULSER No. 2 C-3-1035	
DATE: 12-23-47	DRAWN BY: P. Panagos
CHECKED BY: R. V. S.	



ELECTRONIC COMPUTER PROJECT  
Institute for Advanced Study  
Princeton, N. J.

ECCLES - JORDAN TOGGLE STAGE  
C-3-1041

DATE:  
12-26-47

DRAWN BY:  
P. Panagos

CHECKED BY:  
W. Ware

Consider first the case of negative pulses applied through a capacitor to the grid of the conducting tube. (Negative pulses on the grid of the cut-off tube constitutes a trivial case.) Suppose the rise of the pulse is slow compared to the time-constant of the cross-over network. The circuit will then continually readjust itself to the new voltage conditions imposed on it and when the negative pulse has become large enough, the formerly conducting tube will have turned off and the state will have changed. If the triggering pulse now decays at a comparably slow rate, the circuit will follow back to its original state. If, however, the decay be sufficiently sharp, and if the time constant of the network which supplies the triggering pulse be sufficiently short, compared to the cross-over network, the crossover capacitances will be able to "remember" the changed state and to keep the circuit in its altered condition. Conversely, if the front edge of the triggering pulse is sharp, the capacitors in the cross-over position remember the previous state, and if the drive is released before they have changed, the state will not change. However, if the driving pulse is maintained until these capacitors have readjusted themselves, and then the driving pulse decays at such a rate that the crossover capacitors can continually readjust themselves to the new conditions, the circuit will stay flipped into its new state.

For negative pulses on the conducting grid, then, either the front edge of the pulse must be sharp (back edge slow) and the time constant of the driving network be longer than that of the crossover networks, or the back edge can be sharp (front edge slow) and the input driving time constant shorter than the crossover network. The input capacitor and the stray grid-ground capacitance act as a voltage divider to reduce the amount of signal



which is actually applied to the grid so that the former case is desirable, since it allows a larger value of coupling capacitance.

Consider now positive pulsing of the cut-off grid. If the positive pulse is of such amplitude as to cause the circuit to change state but not of such amplitude as to drive the grid to zero bias, the argument obtains substantially as for negative pulsing of the conducting grid. However, suppose the pulse drives the grid into the positive region. As before, the circuit must be held in the altered state long enough for the crossover capacitances to re-adjust themselves. But, by virtue of the extra voltage on the input-coupling capacity (i.e., the voltage on this capacitor is the original grid bias plus the amount that the grid swings positive), if the pulse decays too rapidly, the driven grid will be returned to a point below that from which it originally started, and unless the time constant of the circuit providing the pulse is less than that of the crossover network, the circuit will flip back. Alternatively, the decay time of the triggering pulse must be suitably slow.

If now positive pulses are placed on the conducting grid, what happens. Off-hand, this would seem not to produce any effect. Its operation depends on the fact that the coupling capacitor from the pulse source into the grid can be charged positively by a positive pulse, by virtue of the diode action of the grid-cathode, and that when the triggering pulse decays to zero, the grid is driven negative; provided that the decay time constant of the input-coupling capacitor is then longer than the crossover networks, the stage will stay flipped. With this case, however, it is no longer necessary to use the crossover capacitors, since it is not necessary to remember the previous state

of the circuit; rather, one element of the toggle (in this case, a grid) is placed at the position at which it is desired to have it after the flipping action is completed, and held there until flipping is completed. The discharge time-constant of this input-coupling capacitor is then dictated by the requirement that it must hold the grid negative until the flipping action is complete which is determined mostly by stray capacitances about the circuit. In fact, these stray capacitances do "remember" the previous state of the circuit, and it is necessary to allow them to readjust to the new conditions before releasing the grid. However, in determining this time constant it is necessary to realize that the coupling capacitor exponentially returns not to the cathode voltage (assuming stage started zero biased) but to the negative voltage at which the grid will eventually settle. The charging of the capacitor can occur quite independently of the operation of the rest of the circuit; the trigger pulse can be arbitrarily short, its only requirement being that it deliver to the capacitor a minimum amount of energy; one would suspect then that the product of pulse width by pulse amplitude (energy) would be a constant for this type of triggering, and in fact this is verified experimentally. The pulse can however, not be arbitrarily long; it must be shorter than the decay time constant of the input circuit. Some small consideration must be given to the fact that the flip action does not commence until the triggering pulse falls, and that the minimum time of reaction is therefore influenced directly by the width of the trigger pulse.

This method seems to be the most advantageous of all methods for triggering through capacitors, the only requirement on pulse shape being that it

have a back edge which is faster than the decay time-constant of the input coupling capacitor, that it contain a minimum amount of energy; and be narrower than a certain maximum width. None of these requirements are particularly difficult to meet and to guarantee. Moreover, it has the advantage that since the decay time-constant of the input-coupling capacitor is desired to be relatively long, this capacitor is large in order of magnitude and therefore, less trigger voltage is lost by voltage divider action between this capacitor and the stray grid-ground capacitance. This method has advantages analagous to that of triggering on the grids through diodes, and in fact, in some sense, it amounts to incorporating the diodes within the tube itself.

For positive pulsing then, either the pulse must meet the specified restrictions as in the case of negative pulsing, if the pulse is applied to the cut-off grid; or the pulse shape can be substantially relaxed, if the pulse is applied to the conducting grid, and advantage taken of the new realization that the crossover capacitors can be eliminated if some element of the toggle is placed in the position into which it is desired to have it be after flipping, held there until flipping is complete, and then released.

Negative pulses can also be applied to the grids through diodes instead of through capacitors. This is a more pure form of the new approach, namely, that the grid is pushed to its new position and then released. As soon as the trigger pulse begins to decay, the diode becomes non-conducting and the grid is substantially released from the trigger circuit. It is only necessary that the diode remain conducting long enough for the flip to complete (for the stray capacitances to readjust). This method involves the addition of two diodes, either vacuum or crystal, and two resistors for the diode returns.

## 1. Binary Counter No. 1

The counter originally incorporated into the Multiplier No. 1 was based on the symmetrically driven toggle; i.e., one in which both input leads are pulsed simultaneously but in which each input lead is effective in influencing the toggle only in every other operation. The input stage and a typical stage, together with the input driving circuit, and the inter-stage driving circuit is shown in Drawing C-3-1042.

The toggle circuit proper is the conventional symmetrical Eccles-Jordan type circuit; and for convenience in obtaining the negative grid return voltage, the cathode is operated the required voltage positive. Symmetrical pulsing occurs by virtue of the common plate impedance (11 K ohms), and requires a negative pulse for operation. With this type of toggle it is essential to have the capacitors shunting the transpose resistors (plate-to-opposite-grid-resistors) in order to effect the flip operation. The input driving stage is a conventional stage, normally cut-off by forced cathode bias, and delivering negative pulses for positive pulses received on the grid. The interstage driver is direct coupled to the  $(n - 1)$  plate circuit, and by virtue of the fairly long time-constant in its own cathode, delivers in the plate a steeply changing wave front which decays to a smaller value as the cathode time-constant relaxes. Ordinarily in high speed (one megacycle) operation, this time-constant is much longer than the recurrence rate of operations, and the plate wave-form consists essentially of rectangular waves. A differentiating circuit couples this plate output to the  $(n + 1)^{st}$  stage to provide the necessary negative trigger. A common impedance is also inserted in the grid-return circuits to provide a clear bus.

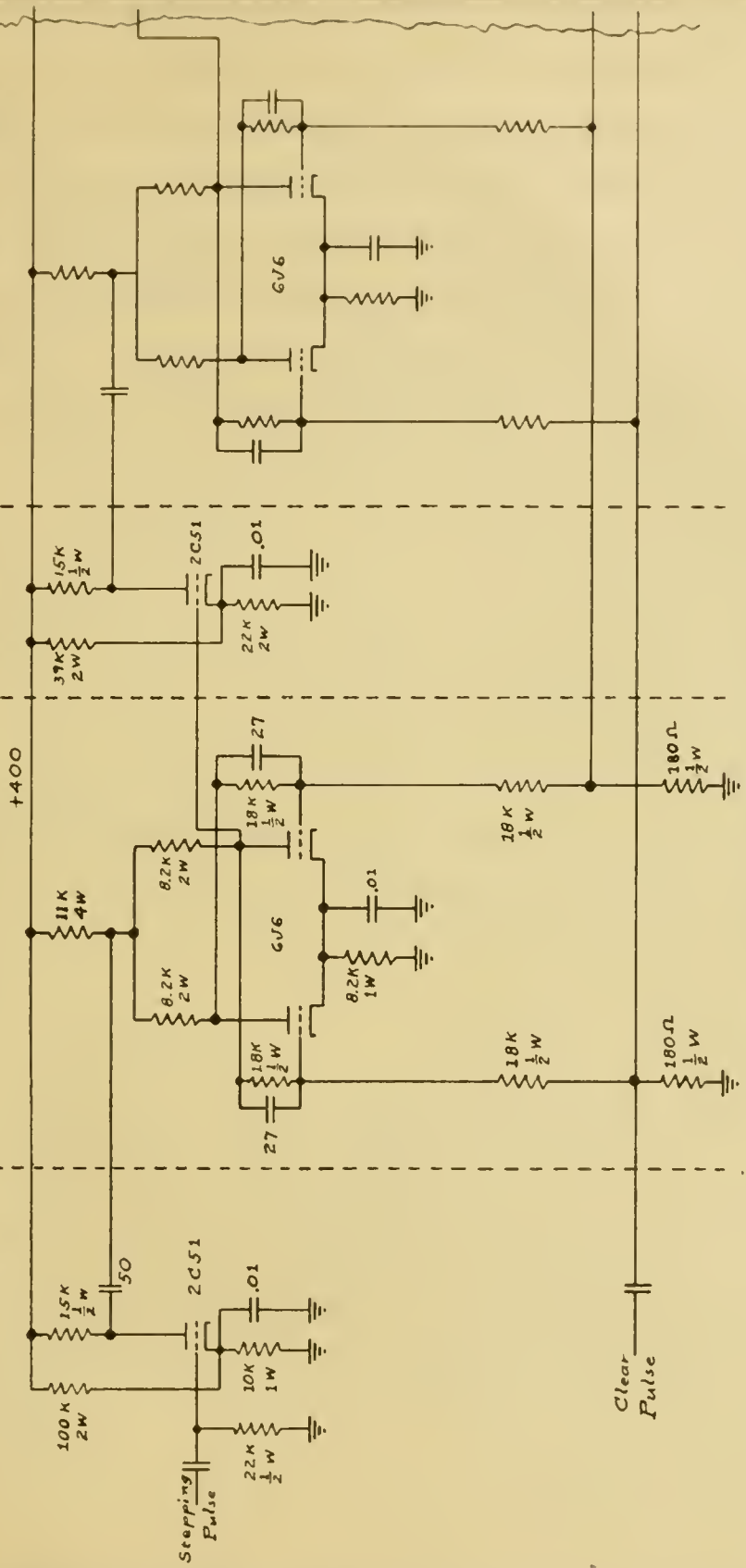


Input Driving Stage

First Counter Stage

Interstage Driver

Second Counter Stage

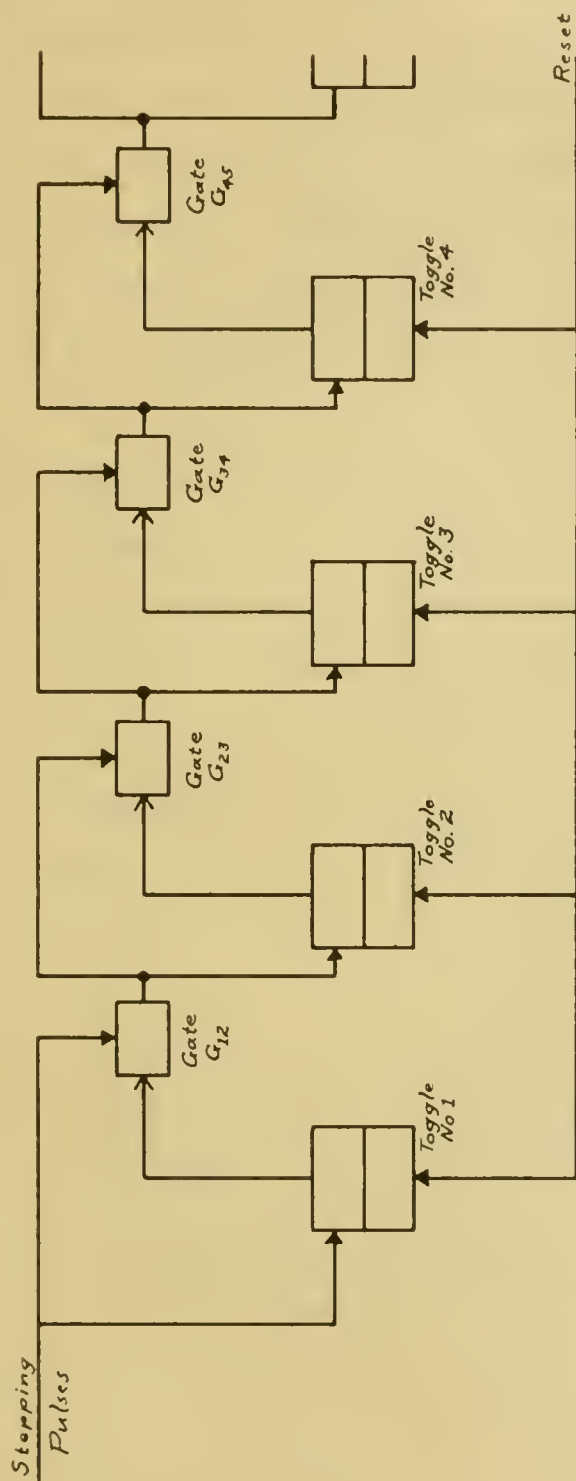


ELECTRONIC COMPUTER PROJECT Institute for Advanced Study Princeton, N.J.		
COUNTER No. 1 C-3-1042		
Date: 12-28-47	Drawn By: P. Panagos	Checked By: W. J. n. l.

This circuit was not reduced to completely satisfactory operation. In the four-stage-counter which was incorporated in Multiplier No. 1, it was not possible to keep all four stages operating simultaneously over an extended period although any one stage might operate for quite a long period. This seemed to be due to the fact that these particular circuit constants were such that the toggle was on the edge of its region of proper operation and small influences were sufficient to throw it out of operation. In addition this type of circuit involving cross-over capacitances as a temporary memory is notoriously sensitive to the pulse shape that triggers it and it is likely this fact caused trouble as well. This latter difficulty can be overcome in principle at least as shown by Drawing C-3-1040. Here a single pulse source which has been designed to provide the optimumly-shaped pulse drives all toggles through gates which operate in response to the states of the various toggle stages. In this case some pulse deterioration could be expected after passage through several gates in sequence, but presumably a proper design could be carried out such that an appropriately-shaped pulse was delivered to each stage.

## 2. Binary Counter No. 2

A second approach to the counter was started along an entirely different philosophy. In line with that philosophy which led to the design of accumulator No. 7 and Register No. 2, it was decided to effect a circuit which was completely binary in the sense that it was completely independent of the shape, rise-time, or duration of input pulse, it only being necessary that the input pulse rise above a certain minimum voltage level and remain there for a certain



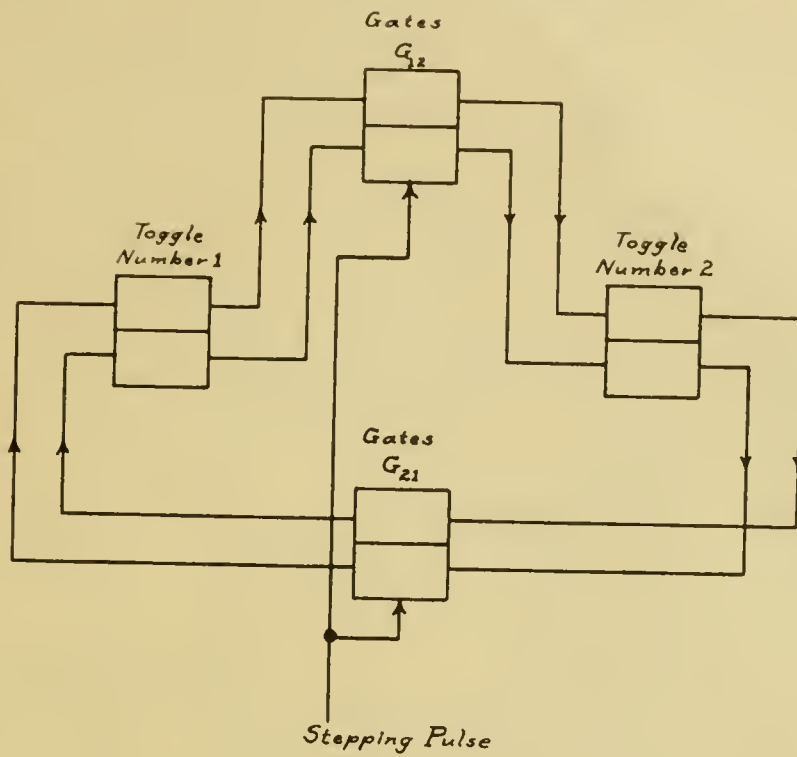
→ D.C. Connection → A.C. Connection

ELECTRONIC COMPUTER PROJECT Institute for Advanced Study Princeton, N.J.		
BLOCK DIAGRAM OF A GATED COUNTER C-3-1040		
Drawn By: P Panagos	Checked By: Whare	

minimum time. To realize this desire required two toggles and two sets of gates as is shown in the block diagram of Drawing C-3-1036. Toggles 1 and 2 may be any toggle circuit, and in this case were selected as Eccles-Jordan type. The interstage gates, or transfer gates, were of the type which influences the toggle circuit by drawing current from the plate circuit. In this type of pulsing, it is not necessary to provide temporary memory of the previous state because a given element is put into the position into which it is desired that it be after the flipping action is completed, and it is held there until the flip action is completed.

The operation of this Counter No. 2 is as follows. One pair of gate circuits (say  $G_{21}$ ) is arranged to be responsive and the other pair ( $G_{12}$ ) unresponsive when the input voltage is at its normal quiescent level. Thus Toggle No. 1 is coupled to Toggle No. 2 through  $G_{21}$  ( $G_{12}$  being ineffective), and because of the transposition in the leads, Toggles 1 and 2 must exist in different states, one abnormal (say Toggle 1) and one normal (say Toggle 2). As the input voltage rises during the pulse, gates  $G_{21}$  become unresponsive and gates  $G_{12}$  responsive. This couples the two toggles together via  $G_{12}$  and causes them to assume the same state; in this example Toggle 2 is assumed to be connected to the plate circuits of  $G_{12}$  and Toggle 1 to the grid circuits of the  $G_{12}$ . Since Toggle 1 is in the abnormal state, it then forces Toggle 2 to assume the abnormal state also. As the input pulse decays, the process reverses itself, and finally as  $G_{21}$  again become responsive, Toggle 2 (in abnormal state) forces Toggle 1 to assume via the transposed connections the normal state. This is recognized as the inverse of the condition that started at the beginning of the pulse, and it is obvious that this circuit will count binarily either toggle providing a rising (or falling) wave front for every other input pulse.



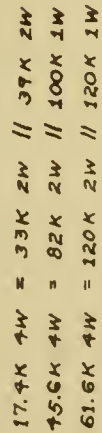


ELECTRONIC COMPUTER PROJECT Institute for Advanced Study Princeton, N.J.		
BLOCK DIAGRAM OF COUNTER No. 2 C-3-1036		
DATE: 12-26-47	DRAWN BY: P. Panagos	CHECKED BY: Ware

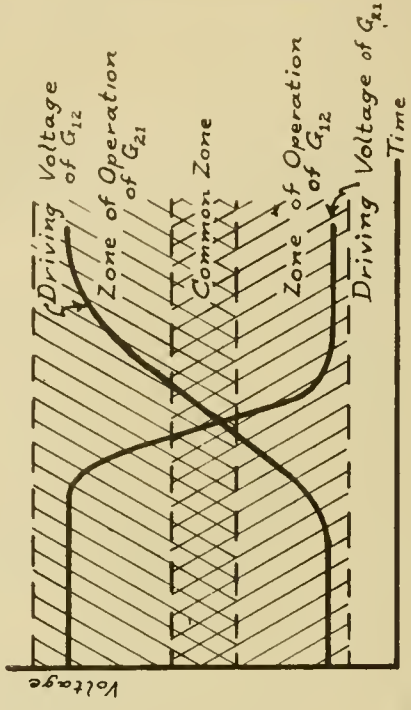
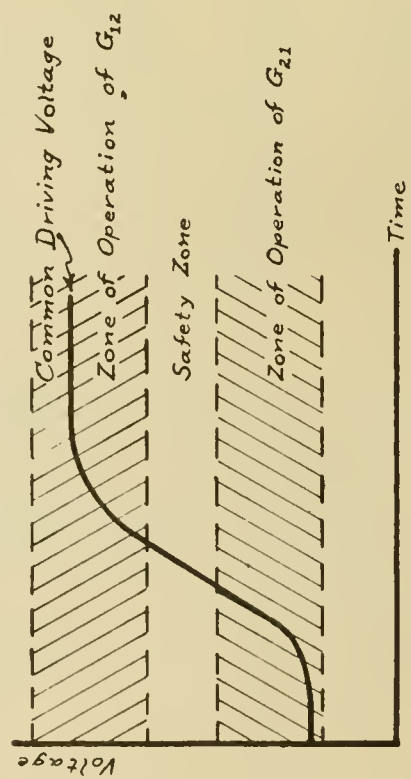
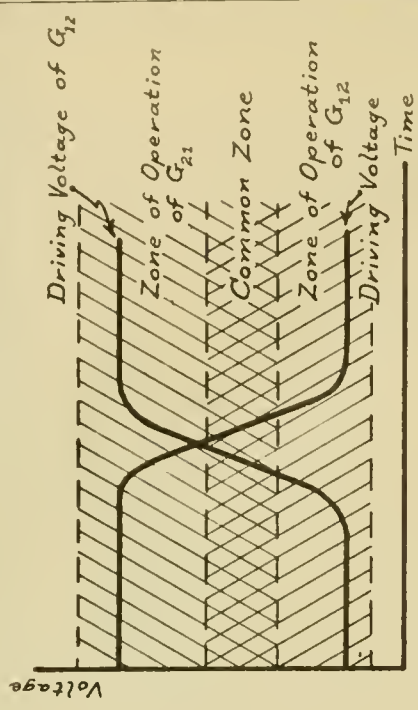
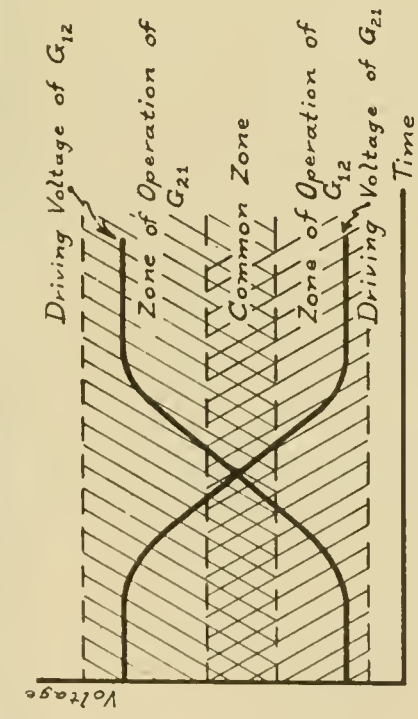
The initial attempt to reduce this circuit to practice is shown in Drawing C-3-1037 and Photograph No. 8. In this circuit, the toggles are conventional Eccles-Jordan type, less the cross-over capacitances which are not here necessary because of the method of triggering, with one grid return available for clearing. The gates are of the twin-triode variety, the common element being the cathode resistor. Obviously if one grid of the combination is sufficiently positive, the cathode will be sufficiently positive that the other triode is cut off, and if this same grid is sufficiently negative, the second section will control. These gates are designed to be driven symmetrically; i.e.,  $G_{12}$  must be driven with a rising voltage while  $G_{21}$  is driven with a falling voltage. To this end, an input stage is provided to pass from a single input pulse to balanced pulses and this is backed up by push-pull cathode followers which are necessary to provide the grid current that these gate circuits normally draw.

This circuit operated successfully pulsewise, but not d.c.-wise. Pulsewise, the circuit at its peak of efficiency, required a pulse of minimum width of approximately 0.5 microseconds and was able to count pulses occurring approximately every 1.2 microseconds. The original design was such as to meet the design criteria described in Section IV.

The cause for the failure of d.c.-wise (arbitrarily slow pulse) operation was discovered and is illustrated in Drawing C-3-1038a. Here is plotted the rising driving voltage of one pair of gates and the falling driving voltage of the other pair, and also the region of operation of the gates.

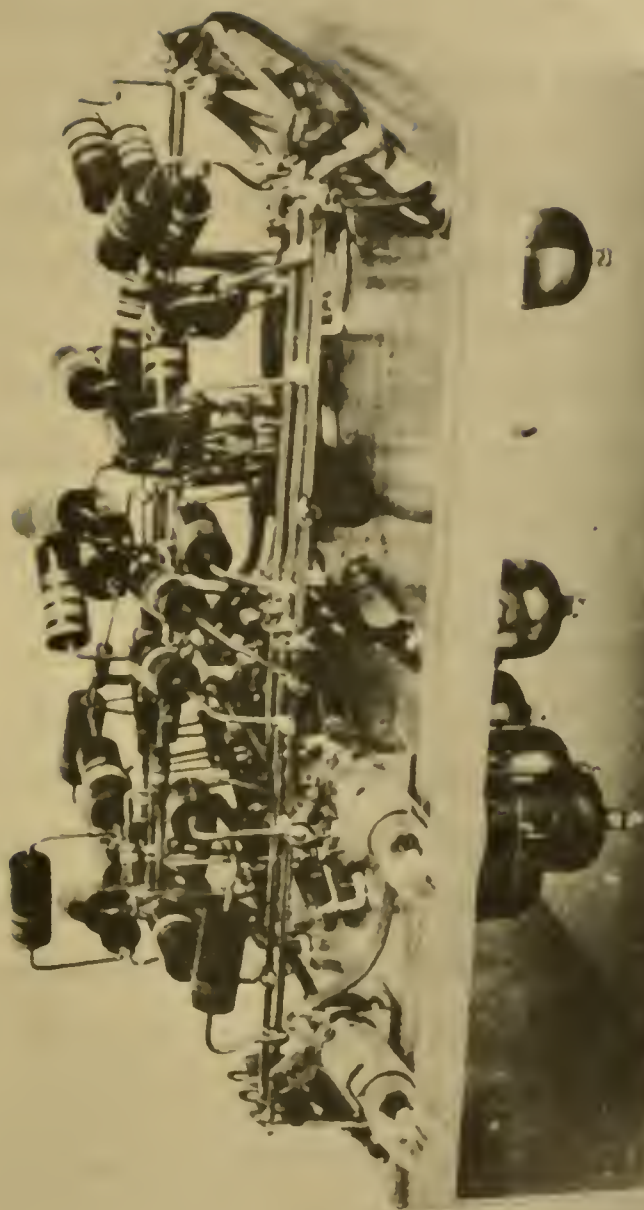


ELECTRONIC COMPUTER PROJECT  
Institute for Advanced Study  
Princeton, N.J.



ELECTRONIC COMPUTER PROJECT Institute for Advanced Study Princeton, N.J.	
OPERATING ZONES FOR COUNTER GATES C-3-1038	
DATE 12-27-47	DRAWN BY P. Panagos
CHECKED BY Whare	





Photograph 8. Binary counter No. 2.

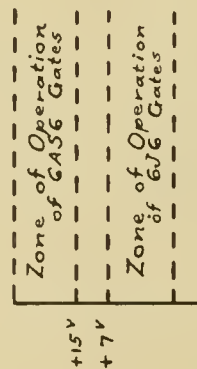
The intersection of the rising and the falling voltage lies within the region of operation of all gate circuits so that there is the opportunity for all four gate circuits to be operating at once, and consequently, depending upon relative strength of the toggles and gates, the circuit will tend to assume a favored position, and not alternate states. This fault evidenced itself in the high speed oscillograms by extraneous peaks and wiggles in what should have been a smoothly changing voltage. The reason for successful pulse operation seems to lie in the ability of the voltages to transit this danger region before any of the gate circuits can act or before the toggle circuits can react. The obvious solution of the problem is to design the circuit such that the intersection of these voltages lies without the zone of mutual operation (see Drawing C-3-1038b). However, should something occur which would cause one voltage to change its characteristic rate of change, the intersection point could very easily drift back into the danger region. For instance, if the circuit were designed properly for d.c. operation, it would also perform for pulse operation, but the addition of sufficient capacity to one of the driving voltages could cause its rate of change to alter to the extent that the intersection point would again be in the common zone. This is illustrated in Drawing C-3-1038-d in which the driving voltage of  $G_{12}$  rises more slowly than in Drawing C-3-1038-b, but the rate of change of the driving voltage of  $G_{21}$  is unchanged.

The real solution of this problem is to activate the two sets of gates with the same voltage, and to stagger the zone of operation such that one falls above the other, as indicated in Drawing C-3-1038-c. In this case it is physically impossible for all four gate circuits to be in operation simultaneously and the circuit is guaranteed against any sort of malfunctioning of the driving pulse. Moreover a specific safety zone can be

established to allow for drifting of operating zones. This requires however, that gate circuits be available which are responsive on negative control voltage, and also gate circuits which are unresponsive on negative control voltage. The twin triode gate fulfills the first condition, and 6AS6 two-control-grid pentode fulfills the second. The realization of this circuit is shown in Drawing C-3-1039. The design is such that it again meets all the severe restrictions mentioned before.

This circuit operates as follows. When the input voltage is quiescent, (-30 volts), the 6AS6 gates are not responsive, and the 6J6 gates are responsive. Consequently, because of the transposition existing between the gates and the two toggles, the toggles are forced to assume opposite states. As the input voltage rises to approximately plus 10 volts, the 6J6 gates are inoperative and the 6AS6 gates are still cut-off (by virtue of the first grid being ten volts negative with respect to the cathode) and at this point the two toggles are independent. As the input voltage continues to rise the 6AS6 gates become operative and the two toggles assume the same stage, Toggle 2 changing to agree with Toggle 1. As the input voltage decays, the 6J6 gates again become operative and Toggle 1 changes to agree with the altered state of Toggle 2, thus completing one count. In this circuit, the 6J6 gates correspond to the  $G_{21}$  gates of the Drawing C-3-1036 and the 6AS6 gates, to the  $G_{12}$  gates.

Admittedly a small amount of time is consumed while the triggering voltage passes through the safety zone, but this is a matter of a few tenths of a microsecond at most, since the safety zone is only of the order of 10 volts wide.



REVISED SCHEMATIC OF COUNTER No.2  
C-3-1039

DATE:	12-27-47	DRAWN BY:	P. Panagos	CHECKED BY:	Edwars
-------	----------	-----------	------------	-------------	--------

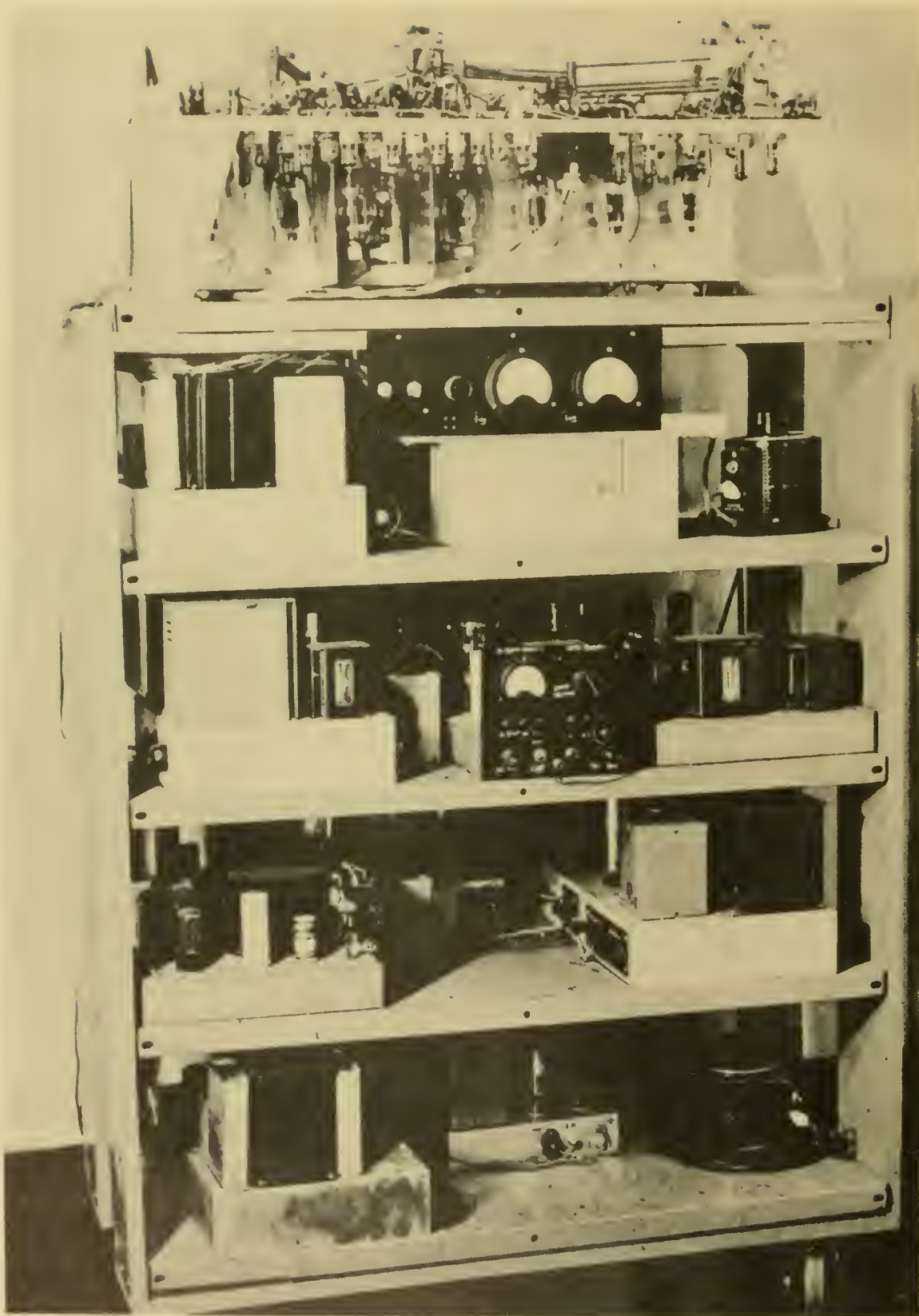
Experimental tests are incomplete on this revision and no results will be stated at this time.

### C. MULTIPLIER NO. 1

For an arithmetic sequence based on Accumulator No. 2 and Register No. 1, a control organ was laid out which would multiply two positive numbers, each of 10-digit length. A block diagram, schematic diagram, and brief outline of its operation is contained in the Progress Report No. 2. In reducing this circuit to proper operation many important design considerations were developed particularly with regard to behavior of adjacent high-current elements (blocking oscillators and high-current cathode followers). The completed Multiplier and its power supply are shown in Photograph No. 9.

Pulser No. 1, described previously, was incorporated six times into the Multiplier No. 1 to provide the necessary shift, clear, and record pulses. A modified version of this pulser using a 6AQ5 oscillator, 6AS6 trigger tube, and a 30 turn - 20 turn transformer was used within the multiplier circuit proper to provide certain high-energy pulses. In the multiplier, the 3E29 output tubes were changed to a pair of 807 tubes in parallel, since it was felt that 807 tubes were manufactured in larger lots and that therefore better control of manufacturing tolerances might prevail. A tremendous difficulty arose when six of these high-current units were connected in a common circuit and physically placed in close proximity. It was necessary to do a herculean task of bypassing and actual shielding to eliminate completely all spurious high-frequency oscillations in the d.c. supply lines and between the oscillators themselves. For instance, in shifting the registers it was necessary to provide a clear pulse followed in 0.05





Photograph 9. Multiplier No. 1 and power supply.

microseconds by a shift pulse. The oscillations accompanying each operation of the clear-pulse source were so severe and persisted so long that the shift-pulse following 0.05 microseconds later was completely lost in the splash that existed in the B-plus 800 volt bus and which was then transferred directly to the cathode output of the shift-pulse generator. The actual precautions were as follows:

- a. A 2 mfd. 1000 volt capacitor had to be provided for every four output tubes, in close proximity to their plates, to provide the large instantaneous current demand.
- b. Parasitic resistors (10 ohms) were inserted in all output tube grids, and in all oscillator and output tube screens; further, the screens were then bypassed directly to ground at the socket with 0.01 mfd. mica capacitors.
- c. In addition to the current-supplying capacitors of (a), 0.01 mfd. mica bypasses were required directly at the plate of each output tube to suppress a very high-frequency parasitic damped-oscillation.
- d. A physical shield had to be erected between every oscillator and its respective output stage in order to suppress a residual coupling between the plate cap of the oscillator (which contained a very large voltage pulse) and the plate caps of the output stages.
- e. frequent bypassing of the bias bus and other voltage buses in the physical proximity of the oscillator and power output circuits was necessary.

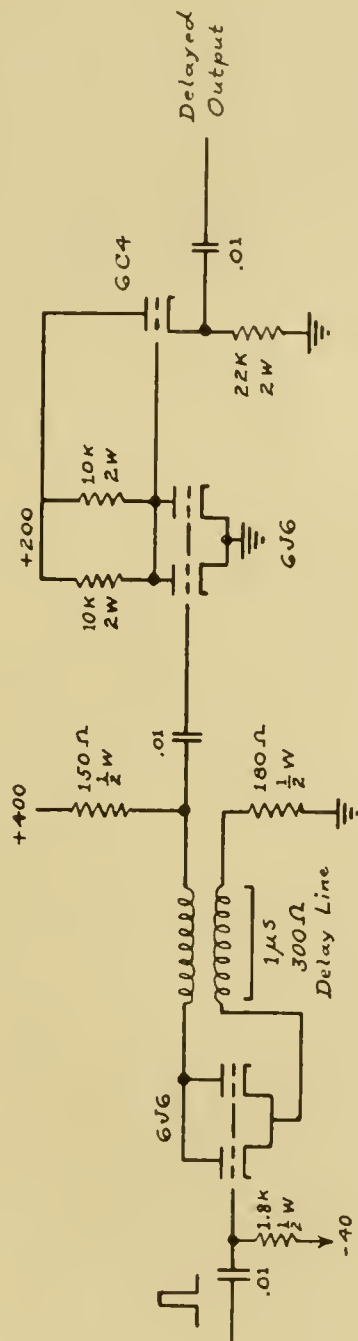
It is interesting to note that the size of the output pulse from all of these high-current tubes was heavily dependent on the heater voltage so that in this respect the design is a faulty one.

In the philosophy of this circuit, there is required an element which will accept a pulse, contain it for a prescribed delay time, and then deliver at the end of this time a pulse with enough power to be reasonably usable. In this circuit, smooth wound delay lines 1 microsecond long were used. As a matter of convenience (forms for unbalanced lines

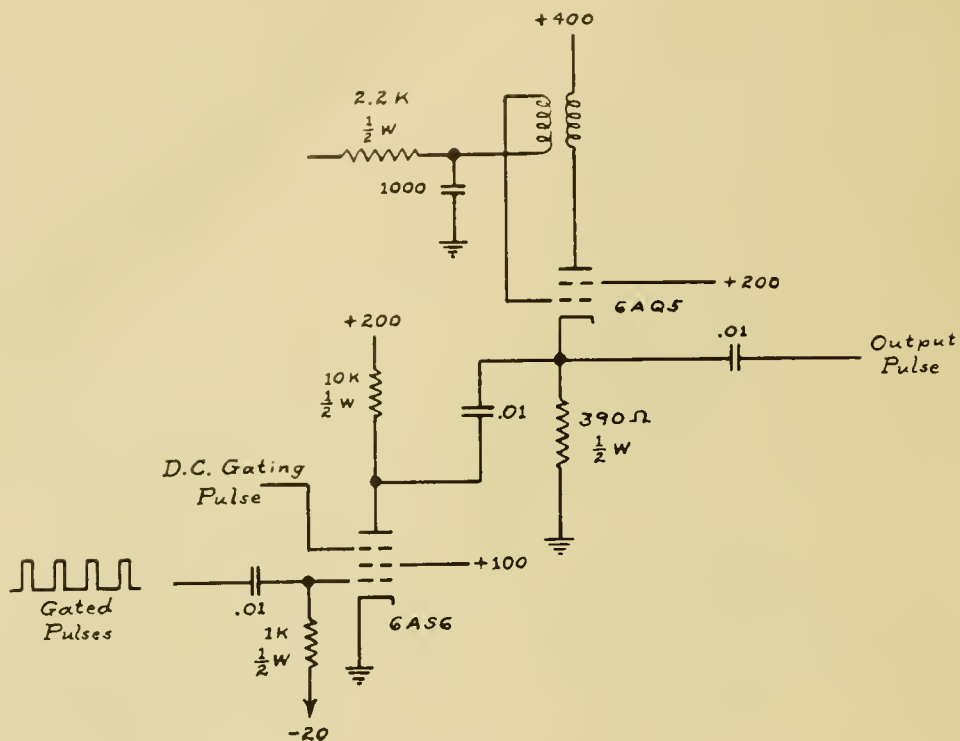
were not available), these lines were all balanced construction so that it was necessary to drive them from a push-pull stage, and unless an automatic 6-db loss of voltage was permissible, to use a balanced receiver. With these very short pulses and steep wave fronts, the attenuation on the lines was very severe, so actually it was necessary to back up the lines with an amplifier stage and cathode follower, the latter because the lines drove circuits which demanded grid currents. An example of this type of circuit is shown in Drawing C-3-1044. A 6J6 served as the balanced driving stage; another 6J6 as the amplifier stage at the output, and a 6C4 as the output cathode follower.

The 0.05 ms. lines were 3 sections of a lumped line and since they were driven directly from the blocking oscillator, and were so short, they provided sufficient output voltage without additional amplification. The gating element of this design consisted of a 6AS6 tube whose two grids are available for the gating and gated function, acting as a trigger tube for a 6AQ5 blocking oscillator. Thus for coincident positive input pulses, a regenerated positive output pulse of standard shape and large output was available. A schematic diagram is shown in Drawing C-3-1043.

With the exception of the counter (described in Section V B) which is necessary in any multiplier circuit, all components of this design performed satisfactorily as indicated in the respective discussions. With the exception of the oscillation trouble of the high-current elements, no particular precaution was necessary to prevent spurious behavior, and this unit would have been capable of driving the Accumulator No. 2 and the Shifting Register No. 1 to the limit of their speed of operation. One microsecond



ELECTRONIC COMPUTER PROJECT Institute for Advanced Study Princeton, NJ		
DELAY CIRCUIT C-3-1044		
DATE: 12-27-47	DRAWN BY P. Panagos	CHECKED BY W. Ware



ELECTRONIC COMPUTER PROJECT Institute for Advanced Study Princeton, N. J.		
GATING UNIT OF MULTIPLIER No. 1 C-3-1043		
DATE: 12-26-47	DRAWN BY: P. Panagos	CHECKED BY: W. Ware



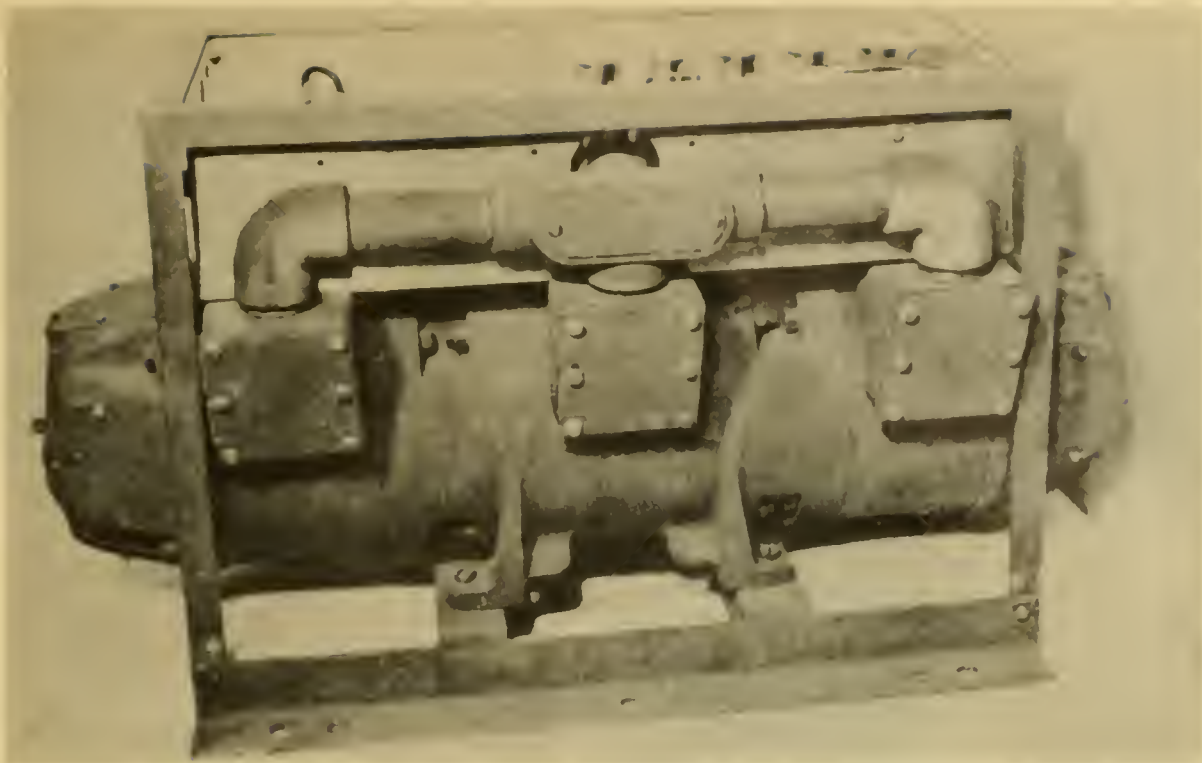
was allowed for each shift, each record, and each clear operation; and for ten stages, one microsecond was allowed for the propagation of a carry. The overall speed of operation then including the reading in of the necessary multiplier and the preliminary clearing of the accumulator would have consumed approximately 35 microseconds for the multiplication of 2 ten-digit binary numbers if the multiplier had contained all digits "one".

## VI. LABORATORY EQUIPMENT

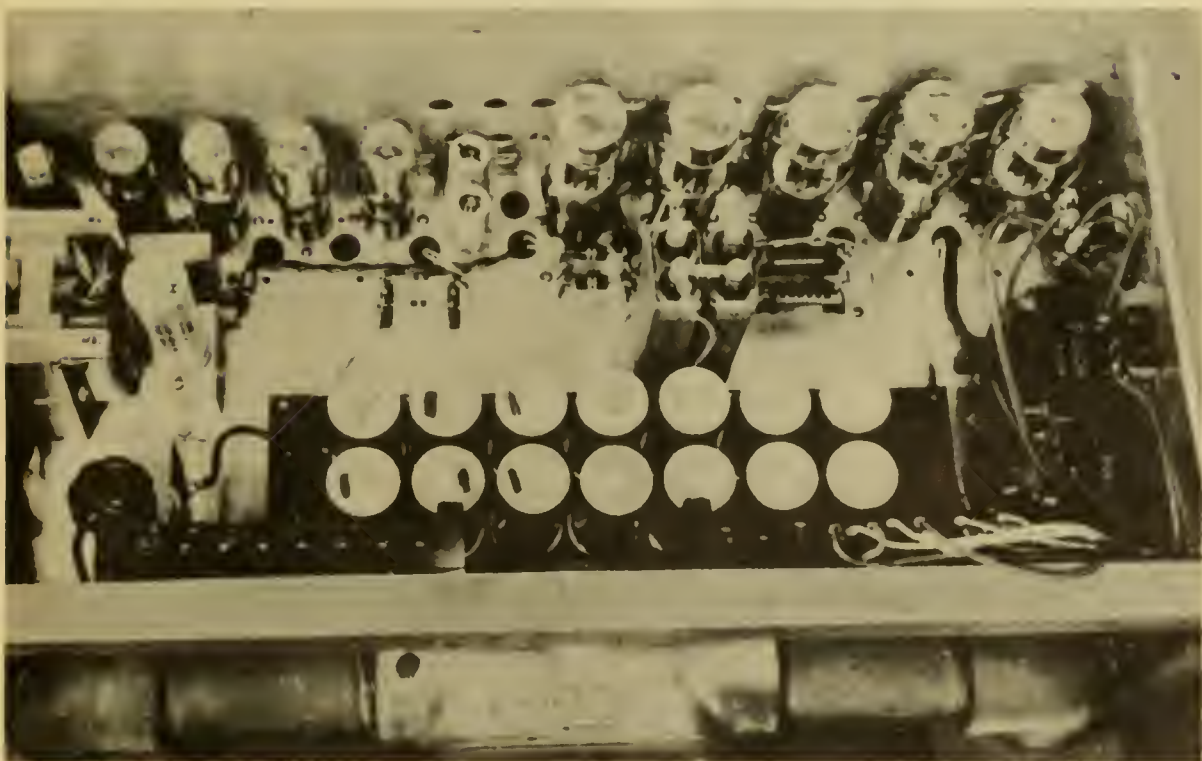
Concurrent with the design and testing work it has been necessary to produce certain additional equipment for the laboratory.

In connection with the work on counters, it was necessary to provide improved amplifiers for additional oscilloscopes. There was an insufficient number of suitable instruments. Inasmuch as a Dumont #241 Oscilloscope had already been converted to triggered-sweep circuits (Progress Report, No. 1) it was decided to alter the internal amplifier to improve its frequency response. Initially, the amplifier was 6-db down in response at approximately 3.5 megacycles, but reducing the plate loads of all stages and altering the series peaking coils accordingly, the response was extended to be flat to 5 Mc. The maximum gain of the amplifier naturally was reduced by this action, but it is still of the order of one volt per inch which is adequate for the work at hand. A suitable low-capacity probe was constructed to work into this amplifier and to provide an attenuation of 10 : 1 with an input capacity of approximately 3 mmf.

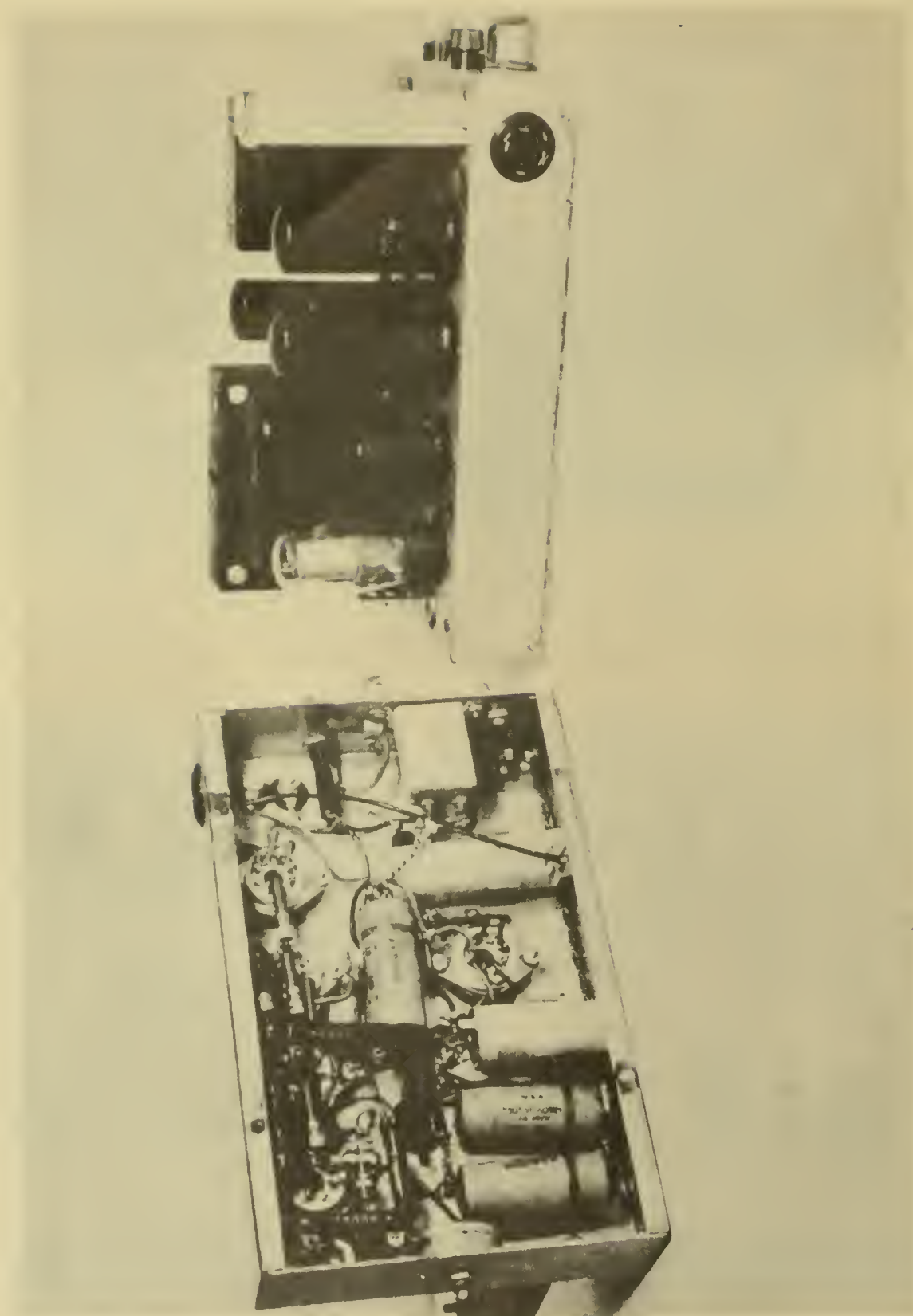
The many supply voltages required by Multiplier No. 1, Adder No. 7, and Shifting Register No. 3 made it necessary to construct a considerable number of regulated power supplies, and to intergrade groups of them into systems supplying the different organs. Photographs and drawings of some of these are shown in the following pages. The circuit of the Sweep, Marker, and Trigger Generator Chassis which was built as an oscilloscope auxiliary is also included.



Photograph 10a. Regulated motor-generator No. 1, general view.

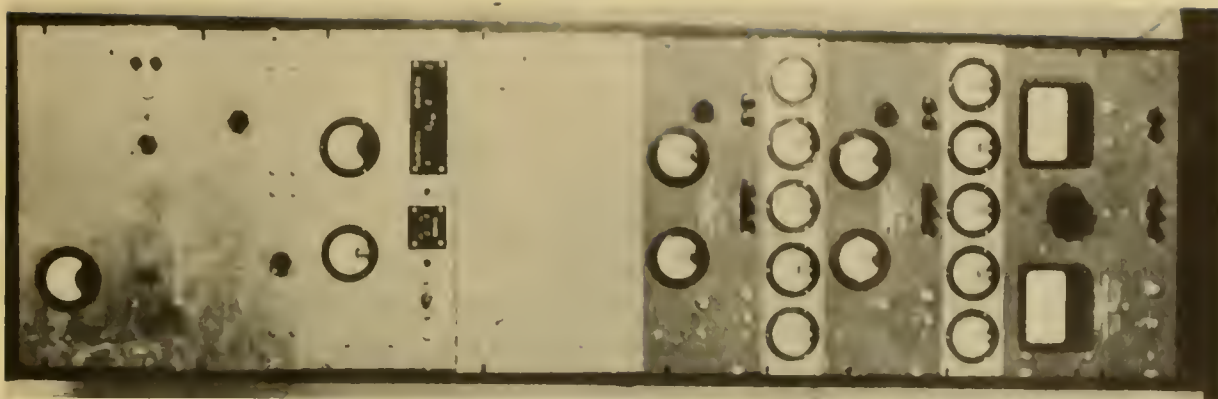


Photograph 10b. Regulated motor-generator No. 1, regulator chassis.

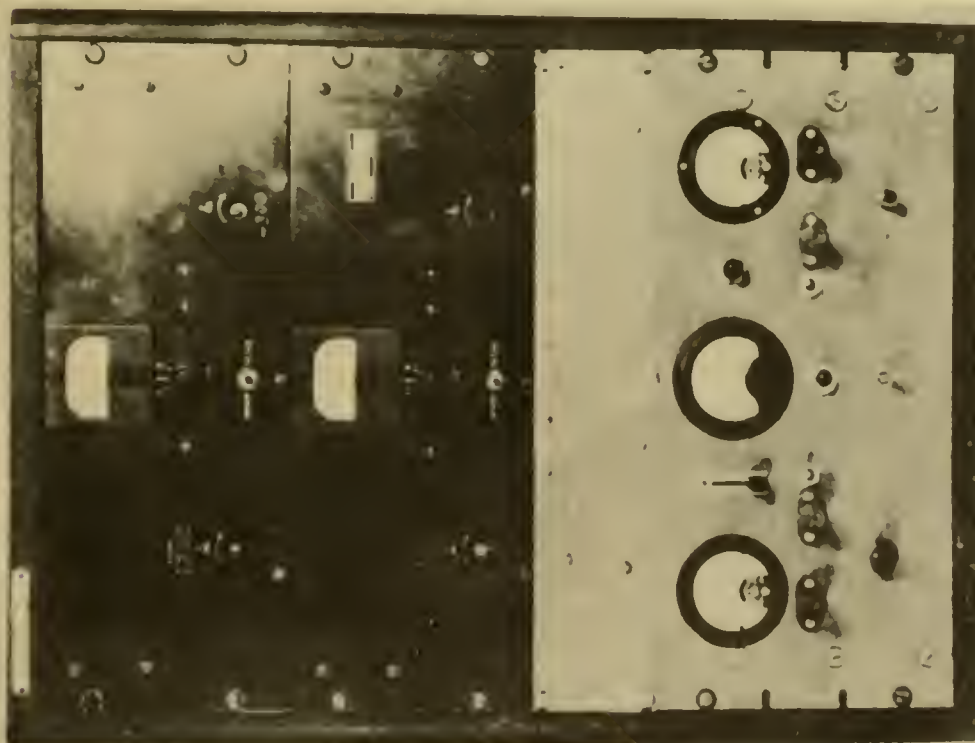


Photograph 11. Converted regulated power supply.



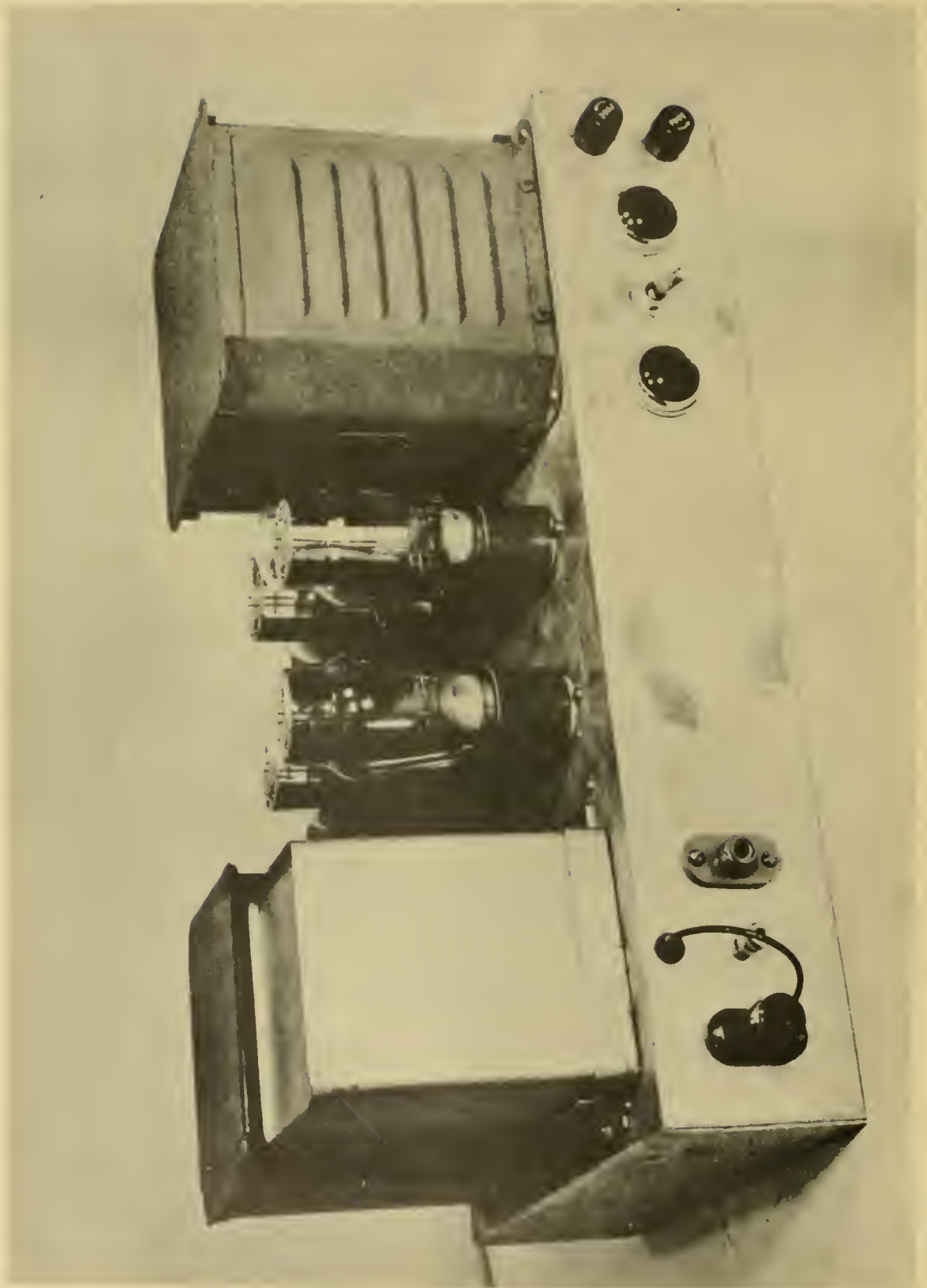


Photograph 12a. Power supply for adding circuits of accumulator No. 7.

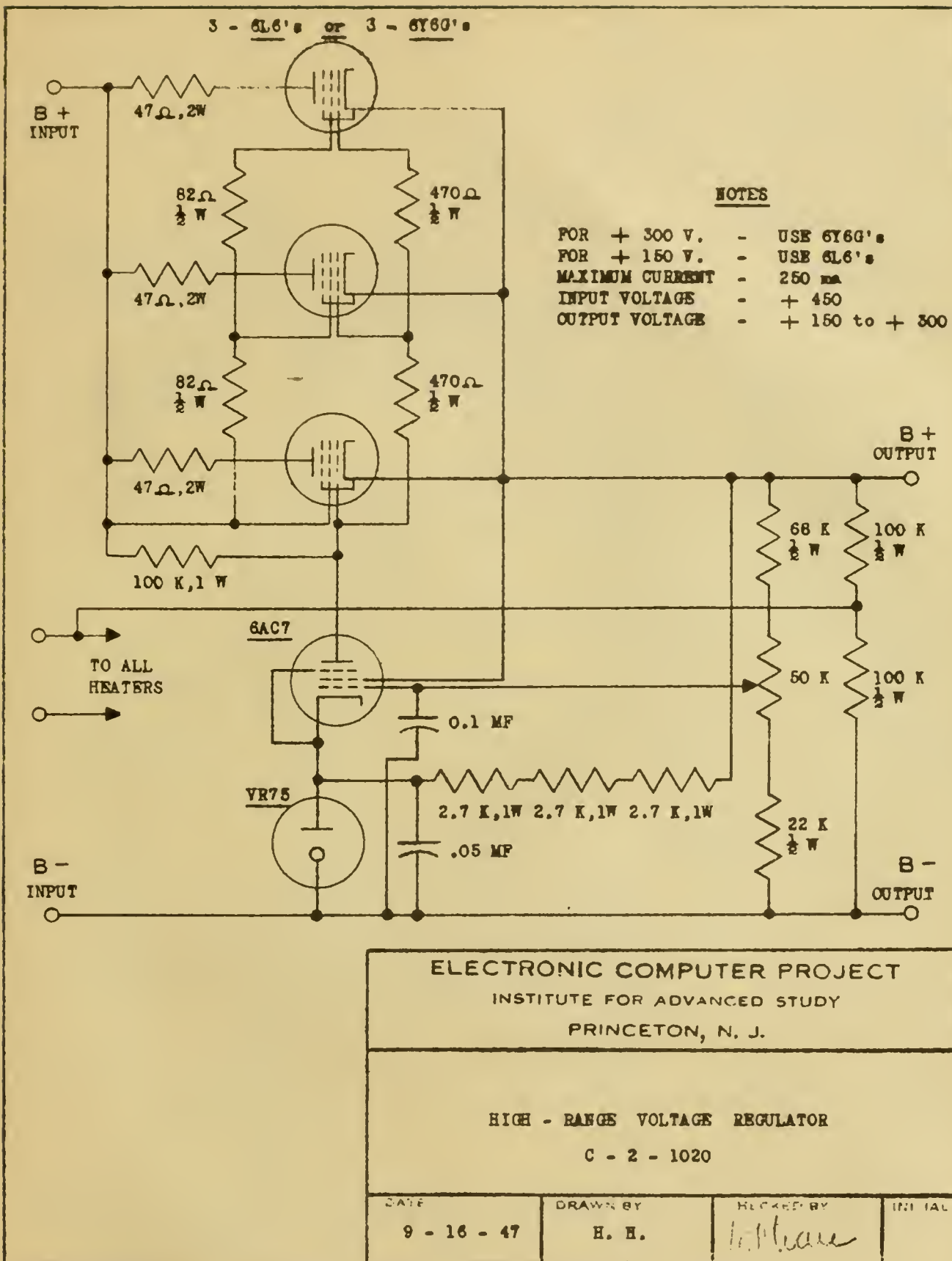


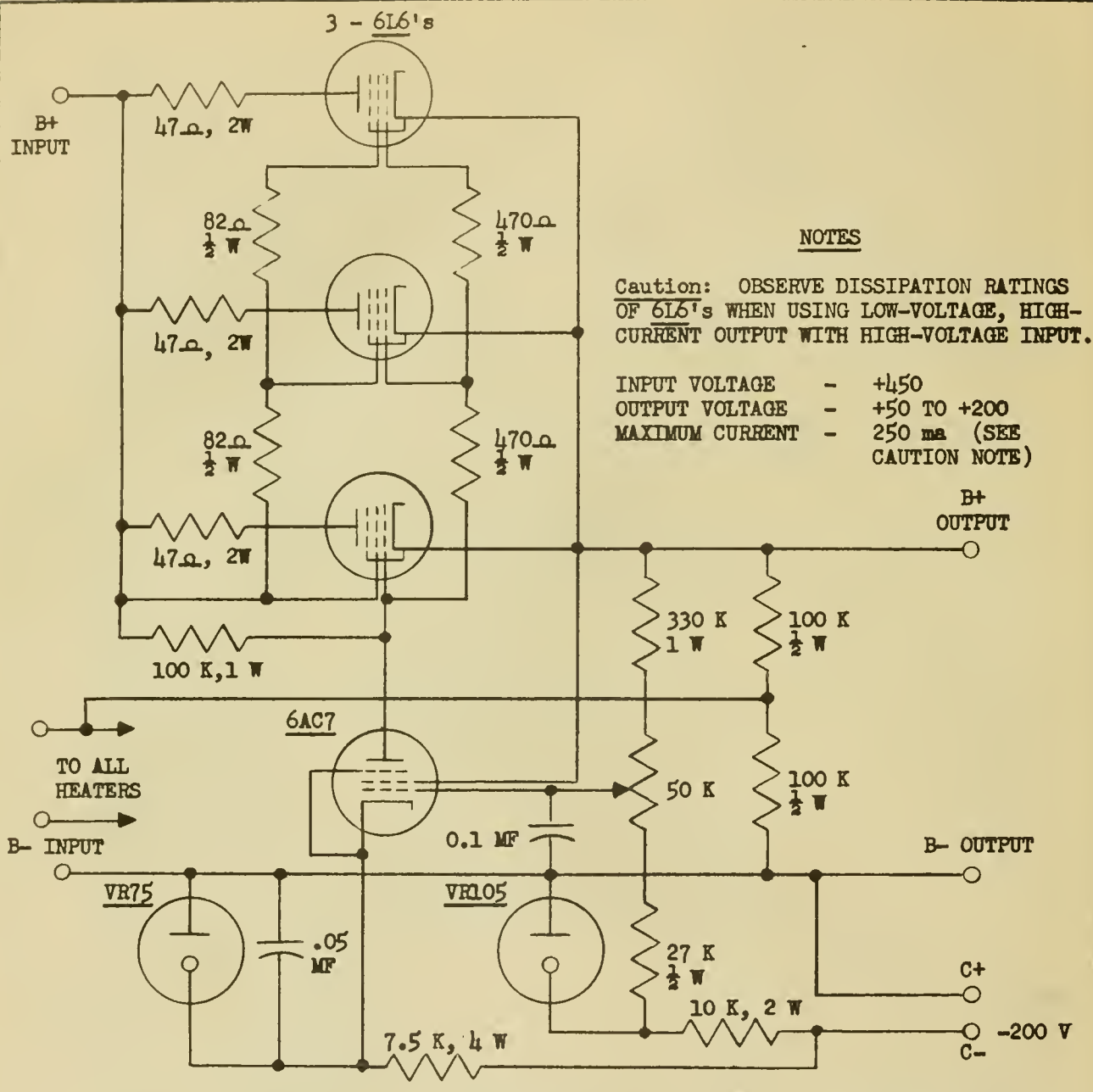
Photograph 12b. Power supply for shifting register of accumulator No. 7.





Photograph 13. 1500-volt, 200-MA. power supply.





# ELECTRONIC COMPUTER PROJECT

INSTITUTE FOR ADVANCED STUDY

PRINCETON, N. J.

LOW - RANGE VOLTAGE REGULATOR

C - 2 - 1021

DATE

9 - 22 - 47

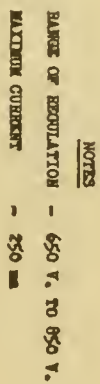
DRAWN BY

H. H.

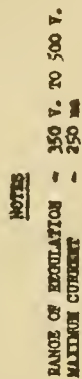
CHECKED BY

W. H. H.

INITIAL



DATE	DRAWN BY	CHECKED BY	INITIAL
9-22-47	H. H.	<i>H. H.</i>	



## INSTITUTE FOR ADVANCED STUDY

PRINCETON, N. J.

## 400 - VOLT VOLTAGE REGULATOR

C - 2 - 1024

DATE	DRAWN BY	CHECKED BY	INITIAL
9 - 23 - 47	H. H.	W. H. H.	

















50 . 2

HS SS LIB  
COMPACT SHELV.

Institute for Advanced Study, Pri

Electronic Computer Project. the

Interim progress report on the

realization of an electronic com

ment by Julian H. Bigelow [and o

Princeton, N. J. ] 1947-

v. illus. charts. (incl.

Various joint authors.

Sixth interim progress report

V. L. Smith has 5 fold. charts

89168

Institute for Advanced Study  
Math. - Nat. Sci. Library  
Princeton, N. J. 08540

